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TECHNICAL MANUAL

MODEL 607 DATA TRANSMISSION TEST SET

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SECTION 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

This manual contains the information necessary to install, operate, and maintain the Model 607 Data Transmission Test Set (DTTS), manufactured by AYDIN MONITOR Systems. The Model 607 DTTS tests, evaluates, and maintains data transmission equipment and systems that operate at bit rates from 10 bps to 100 Mbps.

1.1.1 PHYSICAL DESCRIPTION

The DTTS, as shown in Figure 1-1, is housed in an enclosed chassis that slide mounts into a standard 19-inch (48.26 cm) EIA type equipment rack. Solid state circuitry is employed throughout, with extensive use of integrated circuits for extended reliability. The circuitry is mounted on printed circuit boards, wire wrap boards, and multiwire boards, each connected into the system via cables terminated with dual-in-line connectors or by direct solder connectors.

There are seven subassemblies, labeled A1, A2, and A4 through A8. Five of the subassemblies consist of printed circuit boards, horizontally mounted in the unit; one is a black and white CRT (cathode ray tube) used for displaying setups and results. Boards A5 and A6 are hinged together, making the components of card assemblies A1 and A2 accessible for testing and troubleshooting. Disconnecting all cables from A1 and A2 allows access to power supplies PS1 and PS2. These internal dc power supplies distribute power to the PC boards via barrier strips (TB1 and TB2). Appendix A provides a detailed description of the power supplies.

Input power to the unit is provided by a 115 volt ac line, protected by a 5 amp circuit breaker, ON/OFF switch, mounted on the front panel. The Model 607 DTTS has been designed to minimize the effects of RFI/EMI by the use of a line filter (FL1) incorporated into the ac line. All external signal connections, described in detail in Section 2, are made to the rear panel; all operating controls and indicators, described in detail in Section 3, are located on the front panel. Major components of the Model 607 DTTS are listed in Table 1-1. The subassembly complement is listed in Table 1-2.

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Figure 1-1. Model 607 Data Transmission Test Set

Table 1-1

Major Components of the Model 607 DTTS

Name of Component	Reference Designation	Figure Reference
Control/Display Panel	None	3-1
Rear Connector Panel	None	2-1
Printed Circuit Boards	See Table 1-2	See Section 6
+5/±12 Volt Power Supply	PS1	Appendix A
-4.7 Volt Power Supply	PS2	Appendix A

Table 1-2

Subassembly Complement

Reference Designation	Type	Quantity Used	Functional Name
A1	INFO14-1	1	Interface
A2	PSR024-2	1	Control Processor
A4	CRT	1	Display
A5	GPO29-1	1	ECL Transmitter
A6	GPO31-1	1	ECL Receiver
A7	SM-160	1	Frequency Synthesizer
A8	FPK001-1	1	Front Panel Keyboard
A9	—	1	IEEE: Unit Code Switch

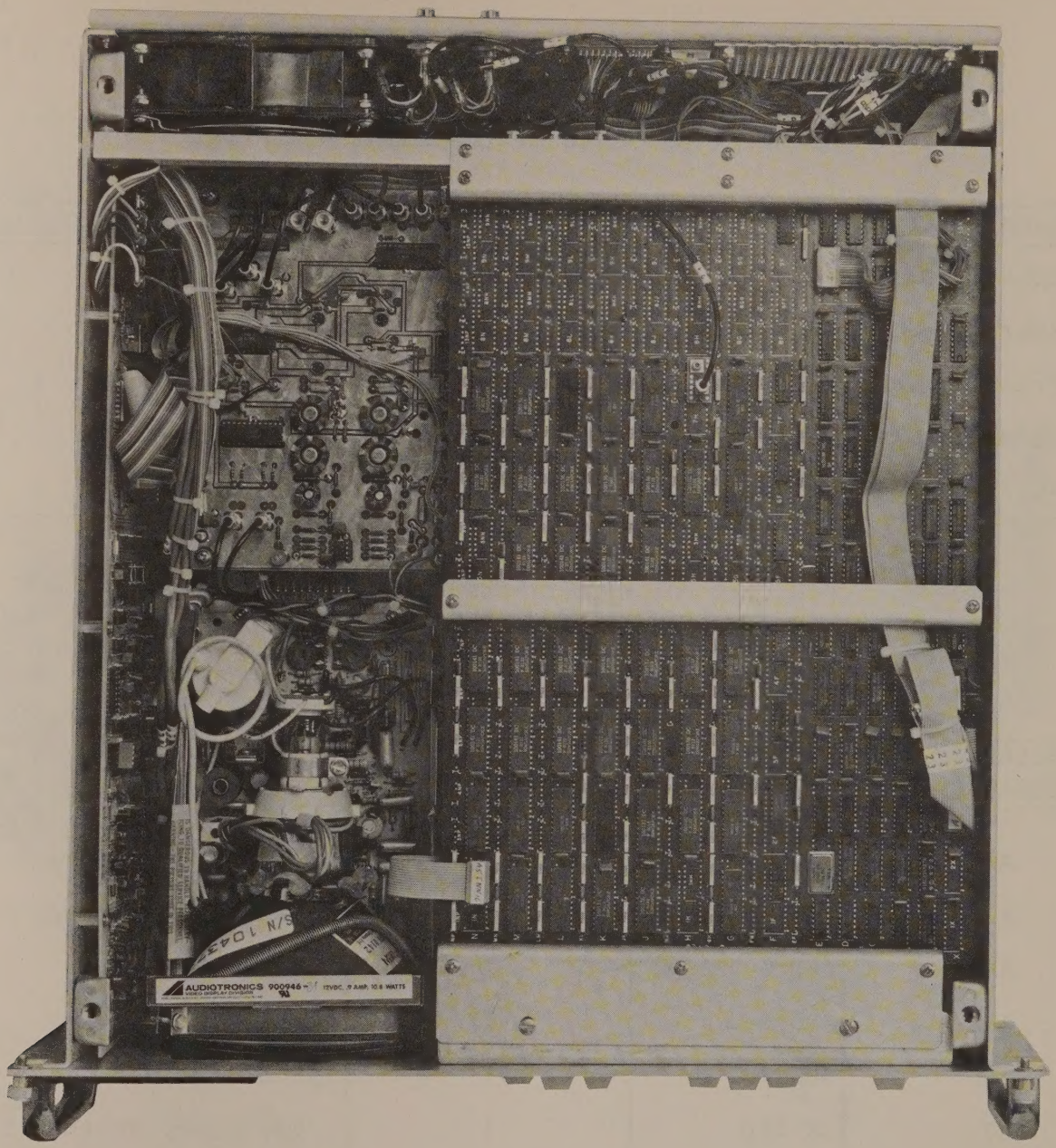

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Figure 1-2. Model 607 DTTS, Top View

1.1.2 FUNCTIONAL DESCRIPTION

The Model 607 DTTS consists of a transmitter and receiver section which are independent of one another. The transmitter section generates data and clock signals which simulate the outputs of data communications source equipment. The transmitter data output consists of one of five pseudorandom patterns or an operator input repetitive pattern. The transmitter clock output is generated internally at a keyboard selectable rate, or externally from a clock signal supplied from a data set.

The receiver section accepts the transmitter clock and data signals as they would be received by data communications terminal equipment. The receiver is capable of reconstructing the same error-free data pattern as was generated by the transmitter section, synchronizing this reference data pattern with the received data, and comparing them on a bit-by-bit basis, in order to detect errors. Accumulated bit errors are displayed on the CRT monitor. Received data bits are counted in blocks, the length of each block being keyboard selectable. Accumulated blocks are counted, and the number displayed on the CRT Screen. The Model 607 DTTS is capable of performing bit error tests of variable time length, the time length in seconds being keyboard selectable. The elapsed seconds and accumulated bit errors are stored and displayed on the CRT Screen.

In block mode or seconds mode, the Model 607 DTTS is capable of detecting, counting, and displaying block errors or second errors, respectively. A threshold of 1-15 errors per block of data (1 to 9,999,999 bits), or per second, must be exceeded to count a block error, or seconds error. The error threshold value is keyboard selectable. Block size is selectable from 10 to 9,999,999 bits below 10 MHz and from 10 to 9,999,999 bits (in 10-bit increments) above 10 MHz.

In the block throughput mode, the Model 607 DTTS counts block errors over an operator selectable number of blocks. After detection of errors, a calculation is performed to yield a throughput rate. The throughput rate is calculated by subtracting the number of blocks in error from the total number of blocks received and dividing this difference by the total number of blocks received. The result is displayed on the CRT, along with a continuous block count and bit error rate. Throughput measurements are made over a test interval of 10^1 through 10^6 blocks, selectable by the operator. In the seconds throughput mode, the Model 607 counts error seconds and continuously calculates and displays the seconds throughput.

If an out-of-sync condition occurs (the true pattern is displaced in time with respect to receive reference generator), such as is caused by a loss of clock, the receiver will automatically resynchronize after the out-of-sync condition passes. The test measurements and elapsed time are halted during an out-of-sync condition. The counting of errors and blocks/seconds is held during the out-of-sync

condition. When synchronization is re-established, the counting continues from the point at which it was held.

Interface selections include differential ECL, TTL, and RS422 inputs and outputs. An IEEE-488 interface bus is used for test result and setup rewording purposes.

A self-test feature is provided on the Model 607 DTTS. In the self-test mode, the transmitter outputs are looped directly to the receiver inputs, bypassing the external interface circuits. This permits all the transmitter and receiver functions within the Model 607 DTTS unit to be exercised without the aid of any external equipment. The transmit interface is still enabled, however, so that the self-test feature also allows monitoring of the local transmitter while it is on line. In the memory test, the microprocessor board performs a CRC on its memory, verifying that all firmware is functioning properly.

The independence of the transmitter and receiver sections of the Model 607 DTTS permits system operation of the unit in simplex, half duplex, or full duplex modes.

1.2 OPERATING REQUIRMENTS

The following subparagraphs briefly cover the operating requirements of the Model 607 DTTS. All general requirements that are normally associated with electronic equipment will apply to this unit.

1.2.1 NUMBER OF STATIONS

The number of stations or installations to be used will be determined by the requirements of the using facility. Each installation at which Model 607 DTTS data is to be sent or received will require at least one Model 607 DTTS unit.

1.2.2 PERSONNEL REQUIREMENTS

The Model 607 DTTS may be efficiently operated and adequately maintained by personnel skilled in electronic technology, and microprocessor circuitry. They should also be familiar with the required data communications equipment with which the Model 607 DTTS is designed to interface.

1.2.3 ENVIRONMENTAL REQUIREMENTS

For most efficient operation, the following conditions are recommended: ambient temperature between 0°C and 55°C; relative humidity of up to 90% without condensation; and at an altitude not greater than 12,000 feet.

1.3 EQUIPMENT CHARACTERISTICS

1.3.1 PHYSICAL CHARACTERISTICS

Table 1-3 lists the physical characteristics of the Model 607 DTTS.

Table 1-3

Physical Characteristics

Parameter	Specification
Width	48.26 cm.(19")
Height	17.78 cm. (7")
Depth	53.34 cm. (21")
Weight	10.8 kg. (23.75 lbs.)

1.3.2 FUNCTIONAL CHARACTERISTICS

Table 1-4 lists the ac power requirements of the Model 607 DTTS (the required dc power is generated internally), and Table 1-5 lists the functional characteristics of the Model 607 DTTS.

Table 1-4

Power Requirements

Parameter	Specification
Voltage	115 ± 10 vac
Frequency	47-63 Hz (single phase)
Power Consumption	300 Watts (approx.)

Table 1-5

Functional Characteristics

Parameter	Specification
PATTERNS	
Pseudorandom	2^9-1, $2^{11}-1$, $2^{15}-1$, $2^{20}-1$, and $2^{23}-1$ bits. Reverse sequence of each of the above patterns. $2^{20}-1$ and $2^{23}-1$ forward pattern zero suppression to limit the number of consecutive zeros in the last two patterns to 14 maximum instead of the normal 19 or 22 respectively.
Repeating Words	Any 2 to 24 bit selected patterns or the following 4-bit words: 1111 (one's). 0000 (zero's). 1010 (dot).
Force	Momentary switch controlled superimposition of one's or zero's over selected pattern.
BIT RATES	
Internal	Keyboard selectable, 5 digits plus exponent through the range of 10 bps to 100 Mbps.
External	Clock input ranging from 10 bps to 100 Mbps.
INTERNAL CLOCK STABILITY	Better than .0025% overall.
TEST MODE	Keyboard selectable, enabling block functions or seconds functions, along with bit error and throughput measurements.

Table 1-5
Functional Characteristics (cont.)

Parameter	Specification
BLOCK SIZE	Keyboard selectable, range of 100 to $1x10^6$ bits/block, 10 bit selectivity above 10 Mbps, restricted to sizes divisible by 10.
TEST PERIOD	2 digits for seconds 4 digits for minutes (up to 24 hours)
ERROR THRESHOLD	1 to 15, selectable per block or per second.
SYNCHRONIZATION	Automatic, using dual register approach. Resynchronizes normally in less than 150 bits with pseudo-random patterns; maintains synchronization at error rates greater than 25%.
DISPLAYS	5" CRT screen
Display Field 1	Blocks or seconds up to 6 digits. Upon overflow changes to 3 most significant digits plus 2 digits of exponent up to a 9.99×10^{99} count.
Display Field 2	Block errors or seconds errors, up to 6 digits. Upon overflow, changes to 3 most significant digits plus 2 digits of exponent, up to a 9.99×10^{99} count. Block or seconds throughput, 5 digit fixed point decimal number. Upon underflow, changes to a floating point decimal. For rates below 1×10^{-2}, changes to 3 digits plus negative 2 digit exponent, down to a 1.00×10^{-6} count.
Display Field 3	Bit errors or bit error probability, up to 6 digits. Upon overflow, changes to 3 most significant digits plus 2 digits of exponent, up to a 9.99×10^{99} count.
Bit Error Alarm Threshold	6 digits or OFF.
Pattern Length	2 digits.
Recirculate Patterns	1 to 24 digits.

Table 1-5

Functional Characteristics (cont.)

Parameter	Specification
Activity Monitors: RD SYNC RT RESYNC ST	Activity on the selected RD, RT or ST inputs to the unit and receiver synchronization conditions are indicated by an asterisk (*) appearing beneath the appropriate monitor field.
Resync Tries	2 digits. Upon overflow, changes to (**).
OPERATIONAL INDICATORS	POWER light indicates system is in operation.
SYSTEM INTERFACE	
Data Outputs SD (Send Data)	ECL-compatible balanced output, TTL output, and balanced E1A RS422 output for transmitter.
Clock Outputs TT (Terminal Timing)	ECL-compatible balanced output, TTL output, and EIA RS422 output for transmitter data rate clock.
Data Inputs RD (Receive Data)	ECL-compatible balanced input, and TTL input.
Clock Inputs RT (Receive Timing)	ECL-compatible balanced input, TTL input, and RS422 input for receive clock.
ST (Serial Timing)	ECL-compatible balanced input, TTL input, and RS422 input for external transmit clock source.
Printer Output	IEEE-488 bus, connected to rear panel; outputs written copy of CRT display.
	RS232 interface (optional), connected to rear panel; outputs CRT display data to RS232 printer.
PR-R	Prints test results and time of day.
PR-S	Prints setup parameters and time of day.
Automatic	Prints at selected interval or on change of status (RD, RT, Sync).

Table 1-5

Functional Characteristics (cont.)

Parameter	Specification
MONITOR PORTS	50 ohms TTL outputs for monitoring interface signals. Useful up to approximately 25 Mbps.
SD (Send Data)	NRZ-L transmit data pattern.
TT (Terminal Timing)	Transmit clock signal with low to high transitions aligned with send data transitions.
ST (Serial Timing)	External square wave clock input to transmitter.
RD (Receive Data)	NRZ-L receive data pattern.
RT (Receive Timing)	Receive clock signal, proper phase has low to high transitions aligned with received data transitions.
INTERFACE SPECIFICATIONS	
EIA RS422	Balanced interface for SD, TT, ST, RD, and RT as supplied through a 37-pin connector on the rear panel in accordance with EIA RS449.
ECL Outputs SDA (J17) SDB (J18) TTA (J19) TTB (J20)	Source Impedance: Two separate 50 ohm transmission lines for TTA, TTB, SDA, SDB. Polarity: Data Binary "1" is a negative level at SDA center conductor. Clock negative to positive transitions of center conductor signal are aligned with data transitions.
ECL Inputs RDA (J21) RDB (J22) RTA (J23) RTB (J24) STA (J25) STB (J26)	Source Impedance: 50 ohm line-to-ground transmission lines. Polarity: Data Binary "1" is a negative level at RDA center conductor. Clock negative to positive transition of center conductor signal is aligned with data transitions.

Table 1-5

Functional Characteristics (cont.)

Parameter	Specification
TTL Outputs SD (J27) TT (J28)	Source Impedance: 75 ohms with short circuit protection. Signal Range: Data Binary "0" + 0.50 ± .5v. Data Binary "1" +3.5 ± 1v. Polarity: Positive going clock transitions are aligned with data transitions.
TTL Inputs RD (J29) RT (J30) ST (J31)	Source Impedance: 75 ohms Signal Range: Data Binary "0" < 1.1v. Data Binary "1" > 1.9v. Polarity: Positive going clock transitions are aligned with data transitions.
TTL Monitor (J1 - J5)	Source Impedance: less than 50 ohms. Signal Range: Unterminated level is 0 to 4 v ± 0.5v. Terminated level is 0 to 2.5v ± 0.5v. Useful bit range, up to 25 Mbps.
SELF-TEST	Transmit data and clock outputs looped back to receive data and clock inputs, bypassing interfaces. The memory on the microprocessor board can be checked.
Insert Error	Injects single error into data stream at a rate (10^{-2} to 10^{-5}) selectable during setup.
Slip Sync	Causes transmit pattern to slip by one bit time.
Interlock	Prevents accidental actuation of insert error function.

1.4 EQUIPMENT REQUIRED

The following paragraphs list the various tools and equipment required for proper installation, operation, and maintenance of the Model 607 DTTS unit. No unique tools or equipment are required.

1.4.1 EQUIPMENT SUPPLIED

Table 1.6 lists the equipment supplied with each Model 607 DTTS unit.

Table 1-6
Equipment Supplied

Nomenclature	Part Number	Qty.
Model 607 Data Transmission Test Unit Top Assembly	356-0026	1
Operation and Maintenance Manual	298-0335	1
Acceptance Test Procedure	297-0647	1
Accessory Kit	354-0149-501	1

1.4.2 EQUIPMENT REQUIRED BUT NOT SUPPLIED

Normal operation of the Model 607 DTTS requires the fabrication of cables for interconnecting the unit to the data communications equipment with which it will be operated. Section 2 of this manual provides fabrication instructions for the cables. Table 1-7 lists the test equipment required but not supplied, and Table 1-8 lists the four basic tools that are required for installation.

Table 1-7

Test Equipment Required

Item	Type	Purpose
Multimeter	Simpson Model 260 or equivalent	Voltage and resistance readings, continuity checks, etc.
Dual Trace Oscilloscope	Tektronix Model 7904 or equivalent	Monitoring waveforms, signals level, etc.
Digital Voltmeter	Fluke Model 8300A or equivalent	Precision Voltage readings.
Electronic Counter	HP5245L or equivalent	Frequency or period measurements.

Table 1-8

Tools Required for Installation

1/4-inch drill with drill set
.100-degree countersink
6-inch flat blade screwdriver
No. 2 Phillips head screwdriver

SECTION 2
INSTALLATION

2.1 INTRODUCTION

This section provides the information necessary to unpack, install, and check out the Model 607 Data Transmission Test Set (DTTS) in preparation for normal operation. Instruction are also included on preparing the unit for reshipment, if required.

2.2 INSTALLATION PLANNING

The Model 607 DTTS is designed for mounting in a standard 19-inch EIA type rack, and requires 7-inch high panel space. Sufficient space must be allowed at the rear of the unit for cabling, and also in front of the rack to allow the unit to be fully extended for maintenance purposes. Further installation planning is determined by the requirements of the using facility. External ac power requirements for the Model 607 DTTS are listed in Table 1-4.

2.3 INSTALLATION LOGISTICS

2.3.1 CABLING

An ac power cable is supplied with the Model 607 DTTS (to J32); all other cables must be provided by the user. Figure 2-1 illustrates the Model 607 DTTS rear panel connector layout. Table 2-1 lists the name, reference, and function of each external connector, and Table 2-2 lists the pin assignments for connectors J7(RS422) and J9.

2.4 INSTALLATION PROCEDURE

The following procedures cover the unpacking of the Model 607 DTTS, the installation of the chassis slide assembly, the mounting of the unit in the equipment rack, checkout of the unit, and instructions for preparing the unit for reshipment, if required.

2.4.1 UNPACKING

The Model 607 DTTS is packaged in a molded foam container within a sealed corrugated carton. To unpack the unit, cut the tape, open the carton, lift off the top half of the foam container, and remove the equipment. Retain all shipping material for possible repackaging and reshipment. Examine the contents carefully for any broken or missing parts, and compare with packing slip for completeness. Report any damage or discrepancies to cognizant authorities for further action.

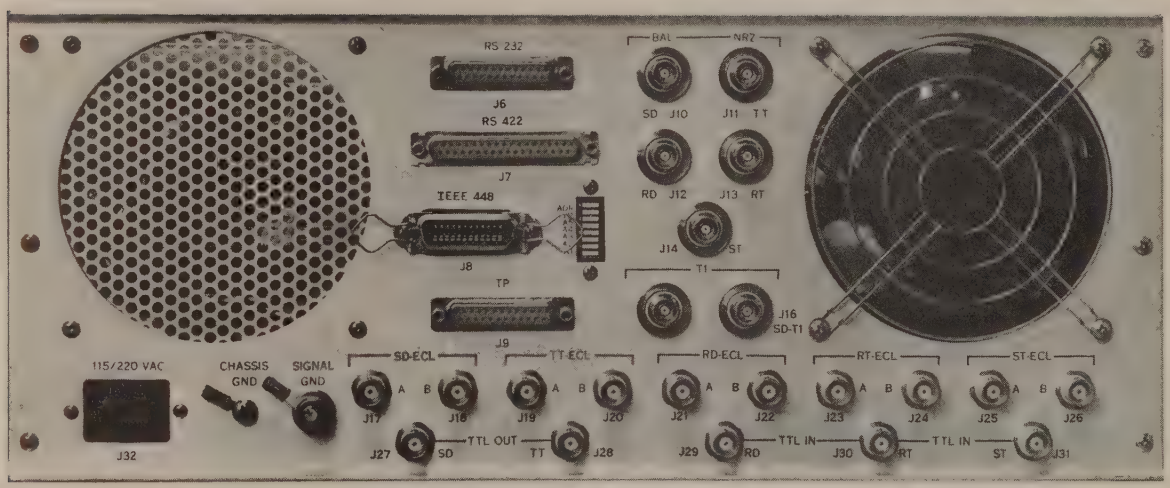

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Figure 2-1. Model 607 Data Transmission Test Set, Rear Panel

Table 2-1

External Connectors

Number	Reference	Function
J6	RS232	(Optional) a 25-pin, ITT DC-25S (or equivalent) receptacle, used for RS232 interface to printer.
J7	RS422	A 37-pin, ITT DC-37S (or equivalent) receptacle, used for RS422 interface signals.
J8	IEEE-488	An IEEE-488 version 1975 compatible receptacle.
J9	TP	A test point mating connector using an ITT Cannon DB-255 plug.
J10 thru J16*	TWINAX	Not Used.
J17**	COAX	SDA ECL balanced output.
J18**	COAX	SDB ECL balanced output.
J19**	COAX	TTA ECL balanced output.
J20**	COAX	TTB ECL balanced output.
J21**	COAX	RDA ECL balanced input.
J22**	COAX	RDB ECL balanced input.
J23**	COAX	RTA ECL balanced input.
J24**	COAX	RTB ECL balanced input.
J25**	COAX	STA ECL balanced input. Not used when internal transmitter timing rates are selected.
J26**	COAX	STB ECL balanced input. Not used when internal transmitter timing rates are selected.
J27**	COAX	SD TTL 75 ohms output.
J28**	COAX	TT TTL 75 ohms output.
J29**	COAX	RD TTL 75 ohms input.
J30**	COAX	RT TTL 75 ohms input.

Table 2-1

External Connectors (cont.)

Number	Reference	Function
J31**	COAX	ST TTL 75 ohms input. Not used when internal transmitter timing rates are used.
J32**	COAX	Power connector, interfaces with supplied power cord.

* Mating connector is TROMPETER PL75-X (or equivalent) TWINAX plug.

** Mating connector is TROMPETER PL20-X (or equivalent) COAX plug.

2.4.2 MOUNTING AND ASSEMBLY

Before mounting the Model 607 DTTS in the rack, the chassis slide assembly should be installed. The only tools required are those listed in Table 1-8. All necessary hardware is supplied.

2.4.2.1 Chassis Slide Assembly Installation. Figure 2-2 illustrates the slide assembly, and identifies the various parts and items called out in the following instructions. To install the slide assembly, proceed as follows (applies to left and right slides):

a. Position the slide fixed front mounting bracket on the rack front riser, so that the lowest mounting hole in the bracket is 2 inches above where the Model 607 DTTS front panel bottom edge will be located.

b. Locate two existing holes in the rack front riser that match the two holes in the slide front mounting bracket.

c. Drill out the two riser holes to 0.219-inch diameter, and countersink (100 degrees) to 0.400-inch diameter.

d. Using No. 10-32 X 7/16-inch screws and nuts, attach the rear mounting bracket to the slide. Rear bracket has slotted holes to permit adjusting for correct length.

e. Attach slide front bracket to rear of rack front riser using No. 10-32 X 1/2-inch flat-head screws and nutbar.

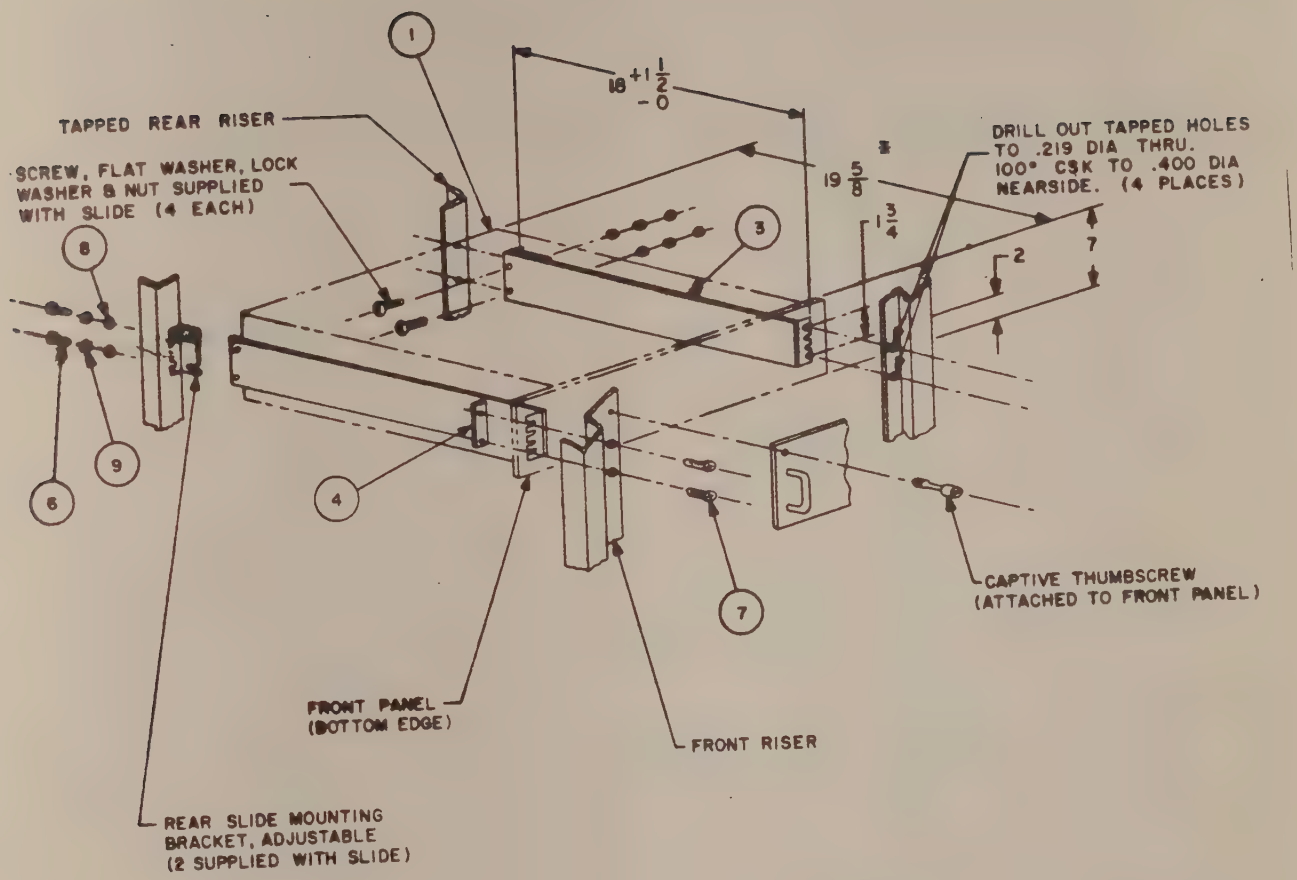
f. Attach slide rear bracket to front of rack rear riser using No. 10-32 X 1/2-inch pan-head screws and washers.

g. Move the slides forward and backward to make certain they move freely.

Table 2-2

Pin Assignments for Connectors J6, J7, and J9

Connector Name	Reference	Pin Number	Function
J6	RS232 Inter-	1	GROUND
	face signal	2	SEND DATA
		4	REQUEST TO SEND
		5	CLEAR TO SEND
		7	SIGNAL GROUND
J7	RS422 Inter-	4	SDA
	face signal	22	SDB
		17	TTA
		35	TTB
		19	SIGNAL GROUND
		8	RTA
		26	RTB
		6	RDA
		24	RDB
		5	STA
		23	STB
J9	Test point	2	SPATSY
	connector	7	BAD BLK
		8	ERROR
		9	RPATSY
		10	RESYNC
		11	ALARM
		12	BLK/SEC INT



‡ INCLUDES RECEPTACLES MOUNTED TO REAR PANEL (NOT MATING CONNECTORS)

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
			LIST OF MATERIALS			
REF	1	20747	356-0086-	———	ASSEMBLY	
	2					
1 PR	3	83508	132-031-004	03000-0[illegible]	CHASSIS SLIDE	
2	4	83508	129-003-001	A300005	NUT BAR, 10-32	
	5					
4	6	96906	127-101-063	MS51958-63	SCREW, PAN HD, 10-32 X 1/2	
4	7	96906	127-105-272	MS24693-C272	SCREW, 100° FL HD, 10-32 X 1/2	
4	8	96906	128-200-808	MS15795-808	WASHER, FLAT, # 10	
4	9	96906	128-202-138	MS35338-138	WASHER, LOCK, SPLIT, # 10	

Figure 2-2. Chassis Slide Installation Drawing

2.4.2.2 Chassis Installation. To install the chassis into the equipment rack, proceed as follows:

a. Pull out the slides until they lock in the fully extended position. Mount the chassis into the slides and slide back until the catch is engaged.

b. Release the catches and gently push unit into the rack until rear of unit front panel is against the rack front risers.

c. Secure the chassis with the two captive thumbscrews located adjacent to the handles.

2.4.3 CHECKOUT AND ADJUSTMENT

The turn-on procedure detailed in Section 3 (paragraph 3.3.1) is recommended as an initial checkout routine after the Model 607 DTTS has been properly installed. No internal adjustments are required prior to placing the equipment into operation.

2.4.4 PREPARATION FOR RESHIPMENT

To prepare the Model 607 DTTS for reshipment, disconnect all cables to the rear panel, and slide the unit out of the equipment rack. Place the unit into the cardboard box, setting it within the molded foam container, saved when the equipment was unpacked. Replace the blue plastic lining, and seal carton securely. Clearly mark the outside of the container as to the contents.

SECTION 3
OPERATION

3.1 INTRODUCTION

The Model 607 DTTS has two basic modes of operation: Setup and Run. In the Setup mode, operating parameters may be changed on the CRT screen. In the Run mode, the unit may be operated either in the block format or seconds format.

This section identifies and defines the function of each front panel control and indicator, presents a recommended equipment turn-on procedure, and details the normal operating procedures for the Model 607 DTTS.

3.2 CONTROLS AND INDICATORS

All operating controls and indicators for the Model 607 DTTS are located on the front panel, illustrated in Figure 3-1. Table 3-1 identifies and defines the function of each control and indicator.

3.3 OPERATING PROCEDURE

Normal operating procedure for the Model 607 DTTS is divided into four specific phases: turn-on procedure, setup parameter selection, testing operation, and shutdown procedure.

3.3.1 TURN-ON PROCEDURE

To initially turn on the Model 607 DTTS unit and check for normal operation, proceed as follows:

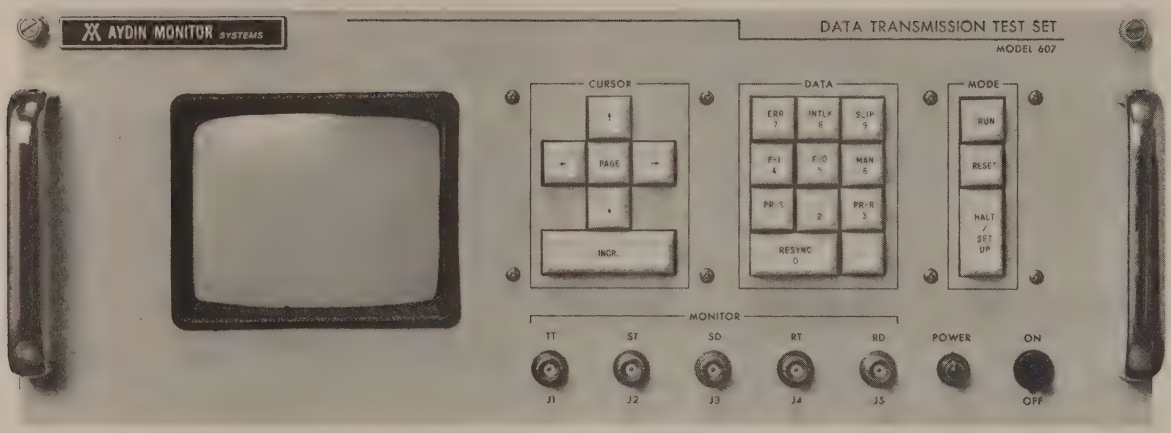
a. Make certain all necessary cables and power are connected to the rear of the unit, as specified in paragraph 2.3.1.

b. Apply power to the unit by setting the power switch to ON position.

c. Observe the following front panel indicators:

(1) POWER indicator illuminated (amber).

(2) Page 2 appears on the CRT screen (after approximately 15 seconds warm-up).



3-1780

Figure 3-1. Model 607 Data Transmission Test Set, Front Panel

Table 3-1

Controls and Indicators

Name	Reference	Function
ON/OFF Switch	S1	Applies ac power to the unit.
POWER Indicator	XDS1	Indicates power is on (amber).
Cursor Control Keys		Positions cursor in display field.
↑		Moves cursor up.
←		Moves cursor to the left.
PAGE		Changes setup pages.
→		Moves cursor to the right.
↓		Moves cursor down.
INCR		Changes character in parameter display fields. Used in Setup mode for non-numeric or tabular selections.
Data Keys (Run mode)		
RESYNC	0	Resets the resync indicator.
PR-S	1	Prints the setup parameters and time of day via the IEEE-488 (RS 232) bus (local mode only).
PR-R	3	Prints the current test results and time of day with headings via the IEEE-488 (RS 323) bus (local mode only).
F-1	4	Force transmission of continuous 1's.
F-Ø	5	Force transmission of continuous 0's.
MAN	6	Force manual initiation of resynchronization of receiver to input data.

Table 3-1

Controls and Indicators (cont.)

Name	Reference	Function
ERR	7	Depress to insert errors in the transmitted data.
INTLK	8	Must be depressed to insert errors.
SLIP	9	Enables the transmitted data to slip by one bit.
Data Keys (Setup mode)	0 - 9	Selects numeric setup values.
Mode Keys		Selects mode of operation.
RUN		Enables test and measurement circuits and corresponding displays and outputs.
RESET		Clears displays and testing results.
HALT/SETUP		Stops testing and enables setup field parameters to be altered.
Activity Monitors	RD,RT,ST, SYNC, RE-SYNC	Indicate activity on CRT screen with an asterisk(*).
Monitor Ports		Valid information up to 25 Mbps.
TT	J1	TTL monitor output of external transmit clock output to rear connector J28, J19, J20, and J7.
ST	J2	TTL monitor output of external transmit clock input derived from rear connectors J31, J25, J26, and J7.
SD	J3	TTL monitor output of transmit pattern provided at rear connectors J27, J17, J18, and J7.
RT	J4	TTL monitor output of receiver clock derived from rear connectors J30, J7, J23, and J24.

Table 3-1

Controls and Indicators (cont.)

Name	Reference	Function
RD	J5	TTL monitor output of received data derived from rear connectors J29, J7, J21, and J2.
IEEE 488 Control	(rear panel)	
A1-A5		Not used in this version of the Model 607.
TO		Enables Talk Only mode of IEEE-488 bus operation.
ADRS		Not used in this version of the Model 607.

3.3.2 SETUP PARAMETER SELECTION

All local operation of the unit is performed using the front panel keyboard and CRT display. The CRT display is comprised of two pages, each containing multiple parameter and test result display fields. All fields and command functions which are user selectable (for example, bit rate) are followed by an underlined group of characters. These characters may be changed using either the INCR key, or a data selection key. To change field selection, position the cursor (blinking underline) to the desired field, using the cursor control keys. Cursor location is indicated by the highlighted area in the display. Enter the selected field, using the data selection keys. If only a fixed set of selections are available for a field, depressing data keys will not affect the display. In this case, depress the INCR key until the desired field selection is displayed. Successive INCR key depressions cause all available field selections to be displayed and cycled repetitively from top to bottom of lists.

Table 3-2 details the range of values permitted for the data selection keys, and Table 3-3 details the selections available to the INCR key fields. Not all of these selection fields are displayed simultaneously. Only those required for the selected test mode (Page 1) are displayed; therefore, it is suggested that the test mode be selected (Page 1) before proceeding with setup parameter selections (Page 2). Any parameter not settable for a particular test is displayed on the CRT as an X.

NOTE

Changing of setup parameters is permitted only in the Halt mode of operation.

Table 3-2

Value Selections for Data Keypad

Field Name	Page No.	Value Range	Function
PAT LEN	1	01-24	Recirculate pattern length.
R/P	1	Any combination of 0 and 1.	Recirculate data pattern.
BIT RATE	2	10 bps - 100 Mbps	Floating point of transmitter bit rate
BLKLN	2	100-1x10^6 (10 bps-9.9999 Mbps)	Block length in bits for low rate.
		100-1x10^6 at 10 bit increments. (10 Mbps-100 Mbps)	Block length in bits for high rate. (Block test mode)
THRS	2	01-15	Error threshold (bits per block/bits per second).
BIT ERR ALARM THRS	2	0-999999 bits	Alarm threshold in bit errors. (Bit Error test mode)
THRPUT TST INT	2	10E1-10E6	Block throughput test interval, # of blocks. (Through-put test mode)
BER TST INT	2	Below 10 Mbps: 10E1-10E10 Above 10 Mbps: 10E2-10E11	Bit error rate test interval, # of bits. (BER test mode)
TSTLN	2	0000:00-9999:59	Test length in minutes and seconds. (Seconds test mode)
TIME	1 and 2	00:00:00-23:59:59	Time of Day HH:MM:SS

Table 3-3

INCR Key Selections

Field Name	Page No.	Available Selections	Function
CNTRL	1	Local	Front Panel operation.
PAT TYPE	1	RECIRC	User defined 1-24 bit pattern.
		PR	Pseudorandom noise data.
		PR REV	Reverse sequence of PR data.
		DOT	Alternate 1/0 pattern.
		ZERO	Constant 0 data.
		ONE	Constant 1 data.
PAT LEN	1	09, 11, 15, 20, 23	$(2^{\text{Pat Len}}-1)$, PR code to be transmitted/ received. INCR Key selection only on PR and PR REV.
ZERO SUPPRESS	1	ON/OFF	$2^{20}-1$, and $2^{23}-1$ codes only.
TX POL	1	NOR/INV	Polarity of transmit data output.
(Test Mode)	1	BLOCKS BLK ERRS BIT ERRS	Block mode.
		BLOCKS BLK THRPUT BER	Block Throughput mode.
		SECS SEC ERRS BIT ERRS	Seconds mode.
		SECS SECS THRPUT BER	Seconds Throughput mode.
BIT RATE	2	10 bps to 100 Mbps	Internal frequency synthesizer, and transmitter bit rate source selection.
		EXT < 10 MB	External clock less than 10 Mbs.
		EXT>/= 10 MB	External clock greater than or equal to 10 Mbs.
INTFC	2	TTL	Up to 50 Mbps TTL.
		ECL	Up to 100 Mbps differential ECL.
		RS422	Up to 10 Mbps RS422.

Table 3-3

INCR Key Selections (cont.)

Field Name	Page No.	Available Selections	Function
TXER	2	OFF, 10E-2, 10E-3, 10E-4, 10E-5.	Transmitter bit error rate.
BIT ERR ALARM THRS	2	0-999999	Alarm enabled. Display reverse-blinks if threshold is exceeded.
		OFF	Alarm disabled
RD and RT	2	NORM/INV	Polarity of receive signals and timing controls.
SLFTST	2	OFF	Off
		LPBK	Internal loopback transmitter to receiver.
		MEM	Memory test.
PRINT	2	OFF	Off
		BLOCK	Prints when block throughput mode is selected at the end of each throughput test interval.
		BER	Prints in seconds throughput mode or block throughput mode at end of test interval.

3.3.3 TESTING OPERATION

To begin testing, depress the RUN mode key, which causes the current operating parameters to be entered into the nonvolatile RAM. Test results will be displayed below the test mode headings on Page 1. Testing may be suspended by depressing the HALT mode key, which freezes the display with the most recent test measurements on the screen. The test measurements may be cleared, or testing halted by depressing the RESET mode key.

Reliable operation of the test set at high bit rates requires that careful attention be paid to clock symmetry and skew relative to data. Clock symmetry must not exceed a 55-45 worst case duty cycle limit. Worst case skew between the clock edge at the center of data bits must be maintained to less than 8% (800 bps to 100 Mbps).

To clear a fault condition, a super-clear feature is available by depressing the INCR, INTLK, and HALT keys simultaneously. The Model 607 will perform a 15-second memory clear cycle, and numeric value display fields which are operator-selectable will appear with question marks or illegal characters. After 15 seconds, all fields should be reset. All key functions are locked out; the clock is halted and increment key selections will go to off. Due to the independence of the transmit and receive sections the transmit function is always active, based on the last setup conditions from the previous Run mode.

3.3.4 OPERATION OF TTL INTERFACE DRIVERS

To use the TTL interface, select TTL on Page 2 of field setup parameters. Monitor the TTL output data (SD) at J27 and timing (TT) at J28 while adjusting R12 and R29 on the INF014 board for the desired level (nominally 2.5v into a 75-ohm load). When not in use, the TTL drivers should be disabled by adjusting R12 and R29 to < 1/2v output. Failure to disable the drivers may result in erroneous test results when using other interfaces.

3.3.5 SHUTDOWN PROCEDURE

To turn the Model 607 DTTS unit off, proceed as follows:

a. Insure that unit is in Halt mode; if it is not, depress HALT mode key.

b. Place the power switch in the OFF position.

c. Observe the following front panel indicators:

   (1) POWER indicator is not illuminated.

   (2) The CRT screen is blank.

SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

This section contains the theory of operation of the Model 607 DTTS. This information, in conjunction with the logic diagrams in Section 6, will enable the user to become familiar with the equipment.

The theory of operation is presented in three levels. The first level is an overall description referenced to the functional block diagram, Figure 4-1. The second level is based on the detailed block diagrams of the circuit boards, and provides a detailed description of each board. The third level is a discussion of the individual subassemblies within the Model 607 DTTS referenced to logic diagrams in Section 6.

4.2 OVERALL FUNCTIONAL DESCRIPTION

Figure 4-1 shows the major functional areas of the Model 607 DTTS. Each block is described in detail in the following sections.

4.2.1 PROCESSOR BOARD, FRONT PANEL KEYBOARD, IEEE-488 PRINTER INTERFACE

The unit is operator controlled, using the front panel keyboard and formatted 5" CRT display. Commands entered by the keyboard are processed by the Z80 processor, which transfers subsequent control bits or setup data to the transmitter and receiver boards. Constructed on a wire wrap socket board, the processor is implemented using predominately TTL logic. Test results accumulated on the receiver or transmitter boards are sampled approximately 60 times per second. The test result data is converted to ASCII, and displayed on Page 1 of the CRT as test results.

Test result data may also be output to the unit's rear panel IEEE-488 or (optionally) RS 232 compatible bus for a permanent, hard copy record of test results. The data output is of the same format as the CRT display. The test configuration may also be recorded using this bus.

Transmitted and received data patterns are controlled using a 16-bit control interface between the processor and transmitter boards. This interface comprises an 8-bit bidirectional data bus, an 8-bit unidirectional control bus, and control signals.

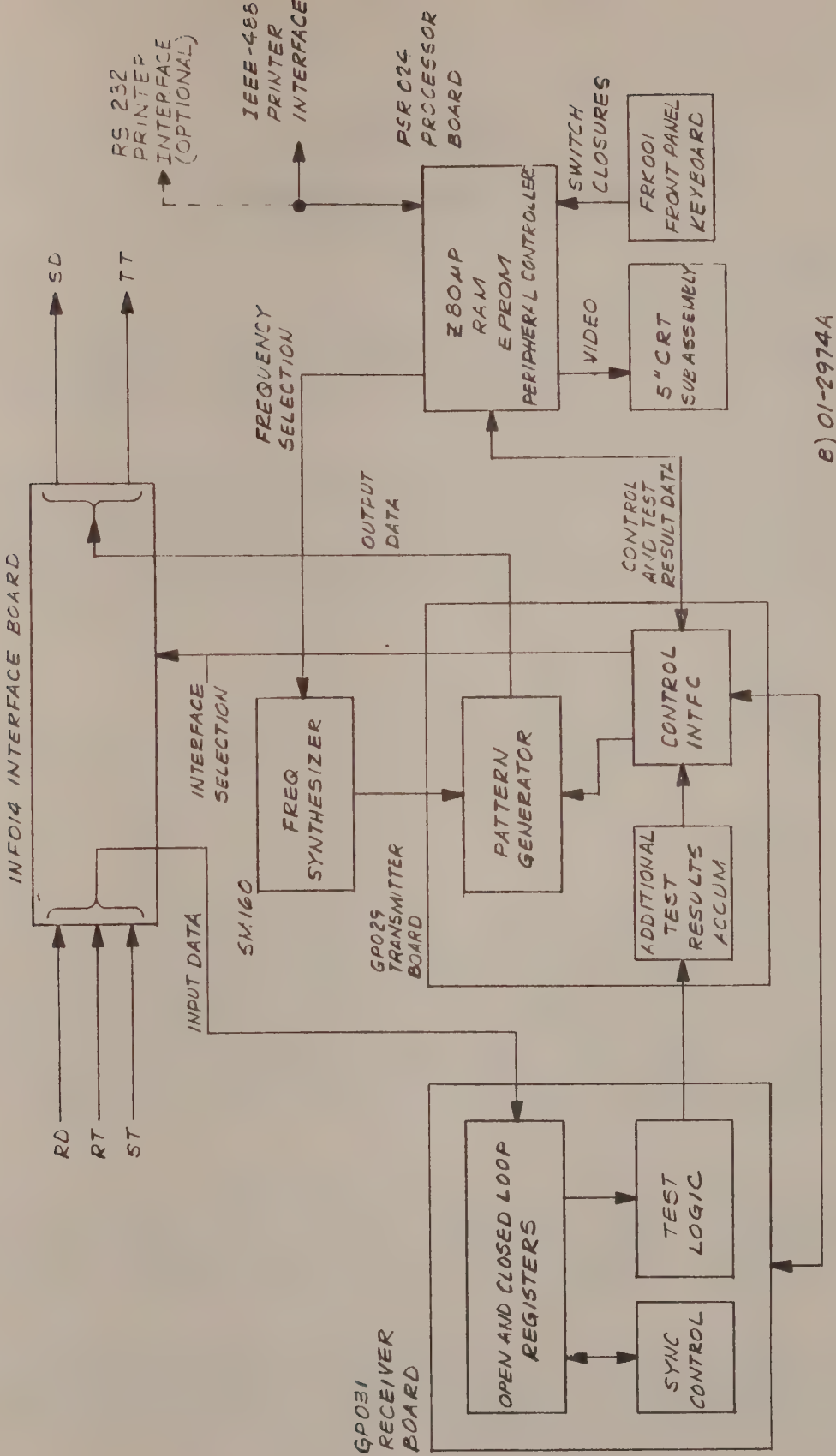


Figure 4-1. Model 607 DTTS, Functional Block Diagram

4.2.2 FREQUENCY SYNTHESIZER

A frequency synthesizer, manufactured by the SYNTEST Corporation, provides a tunable source of transmitter operable bit rate. The module is controlled directly from a 24-bit BCD frequency selection code, held in a processor board register. Output from the module is an ECL level frequency from the range of 20 Mbps to 100 Mbps. Operation of the Model 607 DTTS below 20 Mbps is accomplished using a 20-bit, programmable modulus counter to divide the bit rate of the synthesizer. This counter is located on the transmitter board. For each input of bit rate, selected by the operator on the front panel, the processor board software calculates a combination of synthesizer frequency and binary divisor, which yields the desired transmitter bit rate. The synthesizer rate is loaded into its 24-bit BCD registers, while the binary divisor is loaded utilizing the control interface to the transmitter board.

4.2.3 TRANSMITTER BOARD

The transmitter board generates a serial data stream, selected by the operator. A 24-bit shift register, with selectable feedback taps, generates a variety of Pseudorandom Noise (PN) sequences and recirculated (repeating) patterns. The exact bit configuration for recirculating patterns is selected by the operator using front panel controls. The bit configuration is translated into a 24-bit register pattern by the processor board software, transmitted byte sequentially over the control interface, and loaded into a holding register. The holding register transfers its contents into the pattern generator, after byte transfers are complete.

The transmitter board also contains the control interface for all data and command transfers between the receiver/transmitter functions and the processor card. The transmitter card assembly augments the receiver board's test result accumulation function by containing some counters which could not be physically located on the receiver board. Constructed using a Multiwire ™ baseboard, the transmitter card presents the logic with near constant 50 ohm impedance, interconnecting transmission lines. All pattern generation logic, which operates with clocks as small as 10 nanoseconds, utilizes ECL 100k family devices. These integrated circuits, which are temperature and voltage compensated, along with excellent transmission lines, insure reliable operation of the unit to 100 Mbps. The test results accumulators and control interface logic utilize LSTTL devices. Interface between TTL and ECL utilizes 10k ECL translators, differentially connected to the 100k devices.

4.2.4 RECEIVER BOARD

The receiver board completes two functions; it is responsible for generating a local reference to which the received data is compared, and performing bit error rate, block throughput, and seconds tests. Completing the first function involves synchronizing a local pattern generator to the transmitter generator and allowing for transmission medium delays in the presence of noise. Completing the second function involves accumulating a count of bit or block errors over a period of bits or time.

A local reference is synchronized using a two register approach; an open loop register provides a monitor of the quality of data received from the link, while a closed loop register provides the local reference. A three-leveled synchronization control section constantly monitors the error rates of the received data of both registers, and determines when the local reference is out of sync with the incoming data. When an out-of-sync condition occurs, a resync command is initiated, which requires and error-free sample of the received data to be loaded into the local reference generator for re-establishment of synchronization. Testing is then able to proceed.

The test logic contains test interval counters and bit/block error accumulators. At the end of each test interval, the results are loaded into holding registers, where the appropriate data ready flag is set. The flag, and subsequently the data, is read by the processor board indirectly, via the transmitter board. Two 50-pin ribbon cables connect the transmitter to receiver control and the test results data path.

Similar to the transmitter board, the receiver board is constructed using a Multiwire ^{tm} baseboard. It also utilizes ECL 100k devices for the open and closed registers, and test interval and results prescale functions. After prescaling, the remainder of the test counters is implemented in LSTTL devices. The sync control is also a mixture of ECL and TTL logic.

4.2.5 INTERFACE BOARD

The interface board converts external signal levels to the differential ECL levels, which are used as input to the receiver board and output from the transmitter board. The interface board simultaneously outputs differential 100k ECL and TTL compatible signals. Receivers for 100k ECL, TTL, and RS422 levels are also contained on the interface board.

The source of data to the receiver card is selected on the interface card. Therefore, while all transmitter interfaces are simultaneously active, only one receiver interface may be selected. Selection is regulated by a decoder located on the transmitter board, which is controlled by the processor board. The RS422 output drivers are also located on the transmitter board.

The interface board is a printed circuit card utilizing ECL 100k devices to achieve bit rates to 100 Mbps, a transistor TTL compatible driver for rates to 50 Mbps, and companion ECL, TTL, and RS422 receiver integrated circuits.

4.3 DETAILED SYSTEM OPERATION

This section provides a detailed description of the various circuits within the Model 607 DTTS. Each of the circuit board assemblies references an accompanying detailed block diagram (except for the interface board, INF014-1). In each block of the diagrams, a number, located in the lower right-hand corner, references the sheet number of the corresponding logic diagram, to aid in understanding and troubleshooting the various functions.

4.3.1 PROCESSOR BOARD

Figure 4-2 is a detailed block diagram of the processor board. The Z80 processor controls the operation of the DTTS, and the RAM controls the CRT display data. Each time a key is activated by an operator or the remote control utilized, the Z80 processor reads the commands and places them in the RAM. After processing, the CRT may be updated by the software, the frequency synthesizer rate changed, interface selection altered, or new setup data transferred to the ECL transmitter and receiver boards. While in the Halt mode, the processor scans the keyboard for operator commands. Each input is converted to the internal format and stored in the RAM. When the mode is changed to Run, the processor updates the nonvolatile RAM (NVRAM) with the selected operating parameters, for automatic recall if a power failure should occur. The parameters are then transferred to the transmitter and receiver boards' setup registers.

The transmitter and receiver patterns are only transmitted after a change from the last selected pattern type or operating frequency is made, or upon power-up. When loaded, the transmitter's PN generator is joined with a 24-bit sequence code, which prevents interrupting the transmitter output code and subsequently the receiver synchronization, when not necessary.

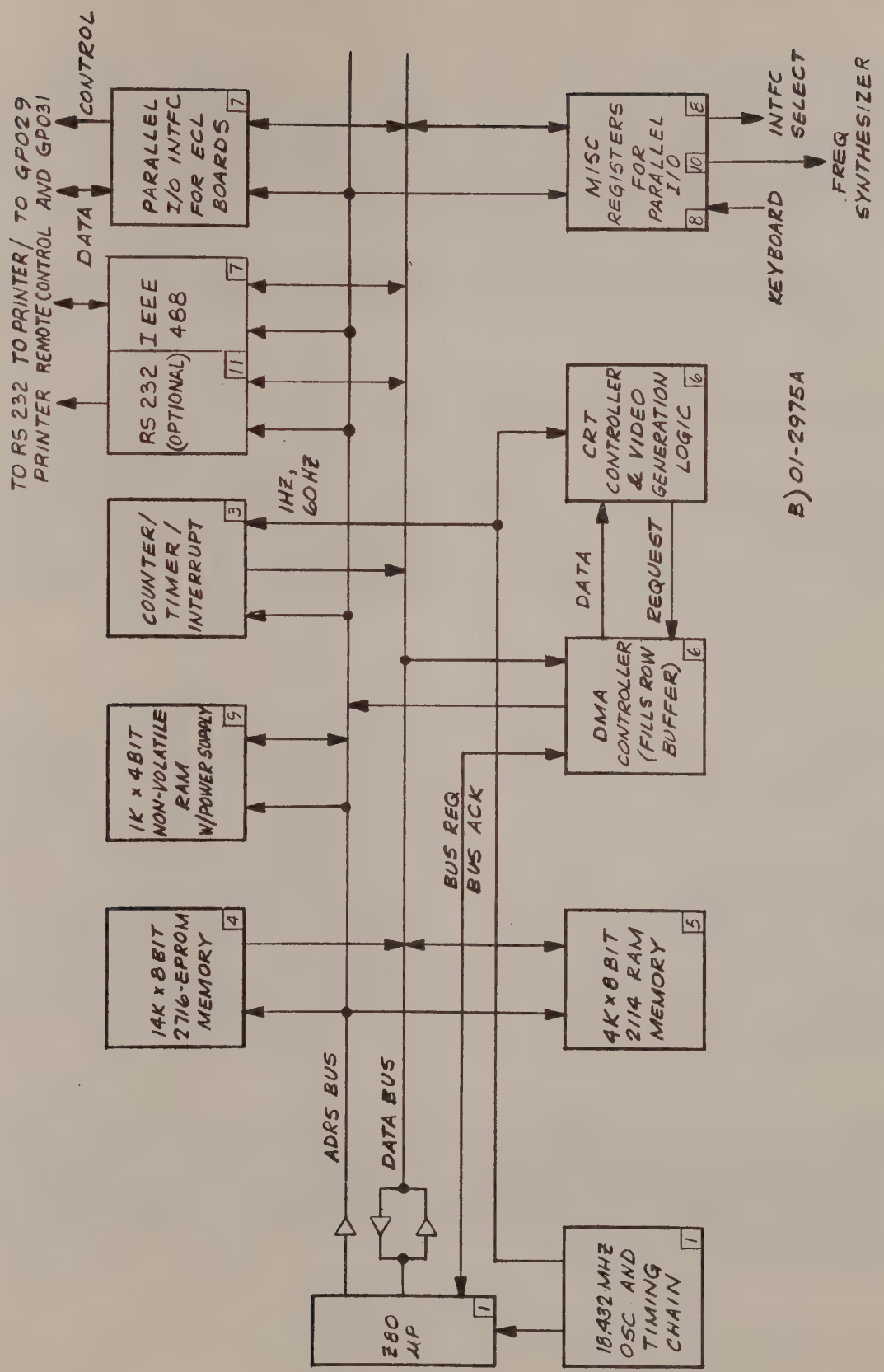


Figure 4-2. Processor Board PSR024-2, Detailed Block Diagram

After all parameters are set up, a RUN TEST command is transferred to the receiver board to begin testing. All of these operations, NVRAM update, parameter transfer, and RUN TEST command, create a noticeable delay between the time the Run mode is displayed on the CRT and when results data appear on Page 1.

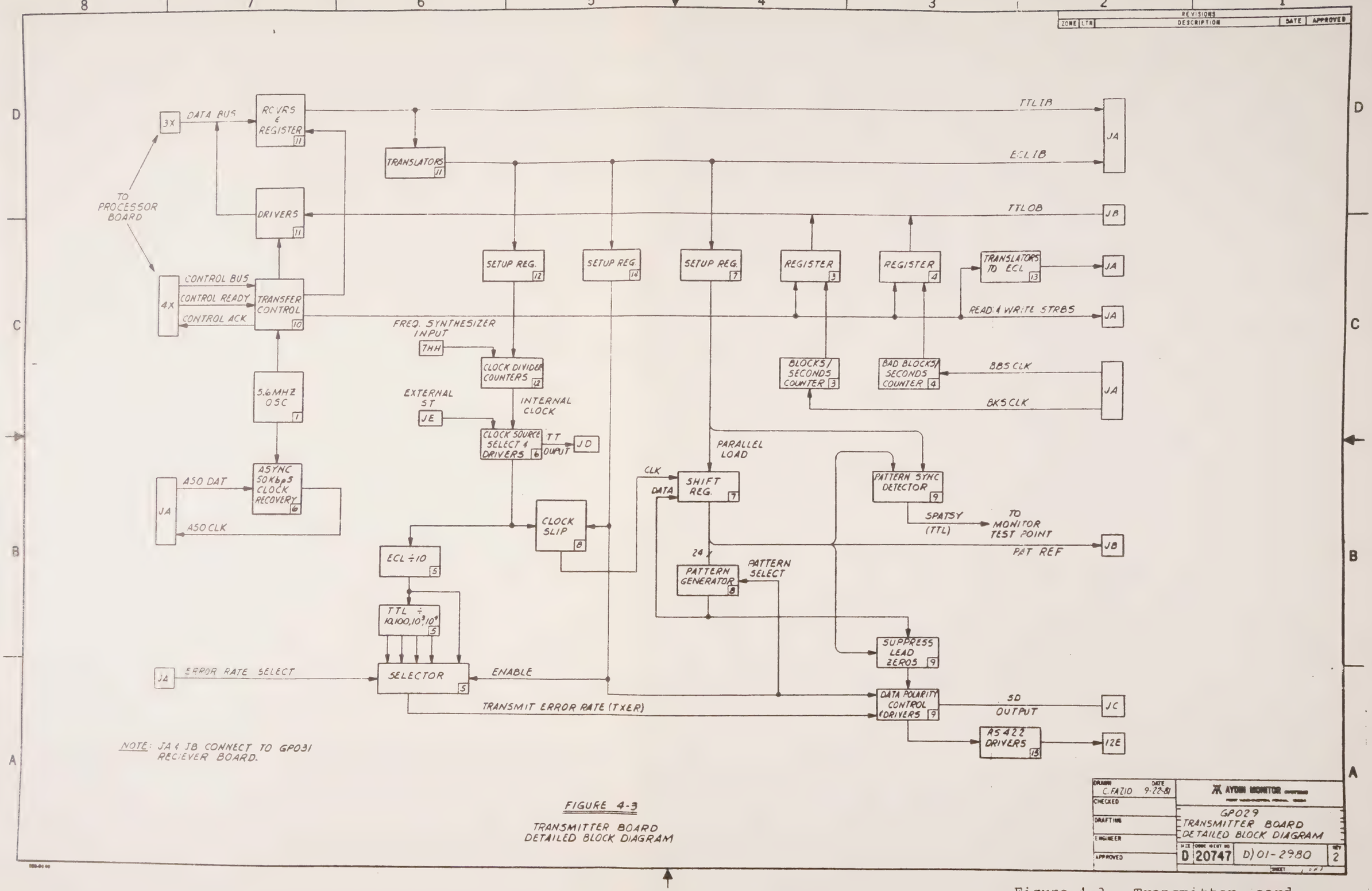
Also during the Run mode, the processor scans the keyboard for additional operator commands, i.e., PR-R or F-1. Each command is interpreted and outputted to the transmitter and receiver boards. Sixty cycles per second interruptions also occur, which force the processor to interrogate the test results accumulator's ready flags. After a test has been completed, the processor issues a latch command, which prevents further updating during readout and moves the test results into the RAM. The latch is negated, and the appropriate calculation routine is executed to generate the required decimal display on Page 1 of the CRT. During the calculation, further 60 Hz cycle interruptions may occur, and operator commands can be acknowledged.

If a print command is received, the processor freezes the display and outputs it on the IEEE-488 bus and, if installed, the RS 232 interface. To prevent loss of data during printing, 60 Hz cycle interruptions are received and new test results are processed, but not displayed. When printing is complete, the CRT is updated to the last stored test results. For special print modes, the processor will initiate a PR-R operation for each occurrence of a bit error rate or throughput test ready flag.

An auxiliary function of the processor board is to record and display the time-of-day on the CRT. This is accomplished by counting 1 Hz cycle interruptions, derived from the processor timing chain and implemented by the counter/timer chip.

4.3.2 TRANSMITTER BOARD

Figure 4-3 is a detailed block diagram of the transmitter board. The transmitter board receives commands and setup data from the processor board, via two 8-bit TTL busses. One bus, control bus (CB), is unidirectional to the transmitter board and contains register address and data direction (Read/Write) information. The second bus, Data Bus (DB), is bidirectional and transfers setup and control information directly to the transmitter board, or indirectly to the receiver board. Test result and status data is sourced by the transmitter board, or indirectly from the receiver board to the processor. TTL to ECL level translators, ECL Input Bus (ECLIB) are used to provide a data path to the ECL setup registers. All status and test result data are contained in TTL registers, and therefore only a TTL Output Bus (TTLOB) exists.



NOTE: JA & JB CONNECT TO GP031 RECIEVER BOARD.

FIGURE 4-3

TRANSMITTER BOARD
DETAILED BLOCK DIAGRAM

DRAWN C.FAZIO 9-22-81	AYDIN MONITOR	
CHECKED	GP029 TRANSMITTER BOARD DETAILED BLOCK DIAGRAM	
DRAFTING		
ENGINEER		
APPROVED	SIZE D	CODE IDENT NO 20747
	D)01-2980	REV 2

Figure 4-3. Transmitter Board GP029-1, Detailed Block Diagram

Setup data is transferred to the transmitter board by the processor. The data is placed on the DB, followed by the destination registers' address on the CB and a control ready strobe. The transfer control logic progresses through logic states based on the 5.6 MHz clock rate, and performs three functions:

- Latches the data into the TTLIB register.
- Transfers the data into the selected setup register.
- Issues a CNTACK reply to the processor to terminate the data transfer.

By issuing a CNTRDY command, data readback is accomplished by the processor setting and address, along with the read line on the CB. The transfer control sequence is as follows:

- Enable the TTLOB to DB drivers.
- Enable the selected register onto the TTLOB.
- Await the negation of CNTRDY, which indicates the processor has accepted the data.
- Disable all drivers.

The primary function of the transmitter board is generating serial data at rates up to 100 Mbps. Data content is operator selectable, and may be parallel loaded into the generator shift register (recirculate mode). Data content is controlled by the processor, which also controls the pattern generator logic for selection of the Pseudo-random Noise (PN) pattern. In the recirculate mode, an ECL setup register is loaded with the operator specified pattern of up to 24 ones and zeros. This data is loaded into the shift register when the following conditions occur:

- Initial application of power.
- Change of pattern or pattern length.
- Change of operating bit rate.

A setup register is also loaded with data to control the pattern generator to act simply as a shift register tap selector for feeding the desired register output. Acting in this capacity, any pattern length (2-24 bits), can be produced repetitively. To guard against an all-zeros lockup state, PN data is generated by parallel loading the shift register with a sequence of PN data, only under the above three conditions. The pattern generator is set up to select the appropriate two

taps required for input to a comparison gate. The modulo-two sum of these taps is fed back to the shift register input, and a series of ones and zeros is generated. The series repeats itself every 2^{N-1} bits, where N equals the longest tap position, i.e., taps 15 and 14 yield a 32,767-bit long pattern. Each time the shift register cycles back to the original parallel-loaded data configuration, a pattern sync detector outputs a pulse, Send Pattern Sync (SPATSY), to the test point connector at the rear panel. This test point provides a convenient synchronization point within the PN stream for oscilloscope observation. Because all test points are TTL level based, operation is limited to approximately 25 MHz.

The rate at which data is generated is controlled by the clock source select logic. External bit rates may be accepted up to 100 Mbps, or an internal clock source may be selected. The internal clock is derived in a series of steps. A frequency synthesizer card, capable of generating 20 Mbps to 160 Mbps is programmed by the processor for an integral multiple of the desired bit rate. The output is received at a connector on the transmitter board, and then inputted to an ECL counter. The counter is programmed to divide the synthesizer rate to the desired bit rate; it is also sized to provide a low end rate of 10 Hz, based on the 20 MHz synthesizer. The selected (internal or external) clock is conditioned by a clock slip circuit before being used by the generator shift register. In the Run mode, depression of the SLIP key, located on the front panel, initiates the following chain of events:

- The processor transfers a control word to the transmitter board, setting the slip bit.
- The clock slip circuit deletes one clock pulse output.
- The shift register appears to slip backward in the output data stream.

The clock slip logic is designed to produce only one clock slip per setting of the slip bit. For an additional bit slip, the operator must release and redepress the SLIP key.

Before becoming output to the external interface, the generated data passes through two additional circuitry functions of the transmitter board. Because certain protocols of data communication equipment prohibit long strings of zeros in data sequences, the PN patterns generated using 20 and 23 bit taps will produce 19 and 23 bit strings of zeros respectively. For these patterns the operator may enable the suppress lead zeros circuitry. This circuit predicts the output data 15-bit times ahead of the actual data, and also counts the number of consecutive zeros. If 15 or more zeros are detected, the actual data is inverted until a logic one is predicted. The operation suppresses (converts to ones) the leading zeros of the zero string.

The data then passes through a polarity select gate to permit operator selection of transmitted data, either normal or inverted. The data is then conditioned by a FORCE 1/0 logic element. Regardless of the transmitter data polarity selected, a constant stream of ones is outputted while depressing the F-1 key, or a constant steam of zeros if depressing the F-0 key.

The facilitate receiver operational checks, a known error rate may be inserted into the transmitted data stream. A five decade ECL and TTL counter chain feeds a selector, whose output is the Transmitter Error Rate (TXER). A setup register on the receiver board transfers the ERROR RATE SELECT signal to the transmitter board via JA. The TXER is used in the data polarity control logic to invert one bit for each TXER occurrence, thus producing transmitted error rates of 10^{-2}, 10^{-3}, 10^{-4}, and 10^{-5}. Although the TXER decade counters are constantly freerunning, the TXER signal is generated only when enabled by a setup bit. This bit is set by the processor board only as long as the operator simultaneously depresses the ERR (Insert Error) and INTLK (Interlock) keys.

The transmitter board also contains some secondary functional sections of the Model 607 DTTS which could not be physcially located with the corresponding primary function. One of these secondary functions is the RS422 transmitter data and clock interface. Another function is the clock recovery circuit for 50 kbps asynchronous data. Receive data in TTL level is routed from the receiver board, designated A50DAT, to the transmitter board. The recovery circuit synchronizes a divide-by-112 counter with the data to produce a 50 kbps clock, designated A50CLK, synchronous with the data.

TTL block and bad block counters, along with their associated registers and control logic, are also located on the transmitter board. The two clock signals, BBSCLK and BKSCLK, are transmitted to the board for counting and readout of total blocks, total blocks/seconds in error during a throughput test, or for use as a freerunning bad blocks/seconds accumulator.

4.3.3 RECEIVER BOARD

Data and clock are selected via two sources: internally, loopback from the transmitter board, or externally, directly from the interface board. The following description of the receiver board details the data and clock activity monitors, along with the alarm circuitry. These circuits, which are connected to the rear panel of the Model 607 DTTS, signal loss of data or clock. The activity monitors also function as input to the status register, which is interrogated by the processor board via the TTL Output Bus (TTLOB). Figure 4-4 is a detailed block diagram of the receiver board.

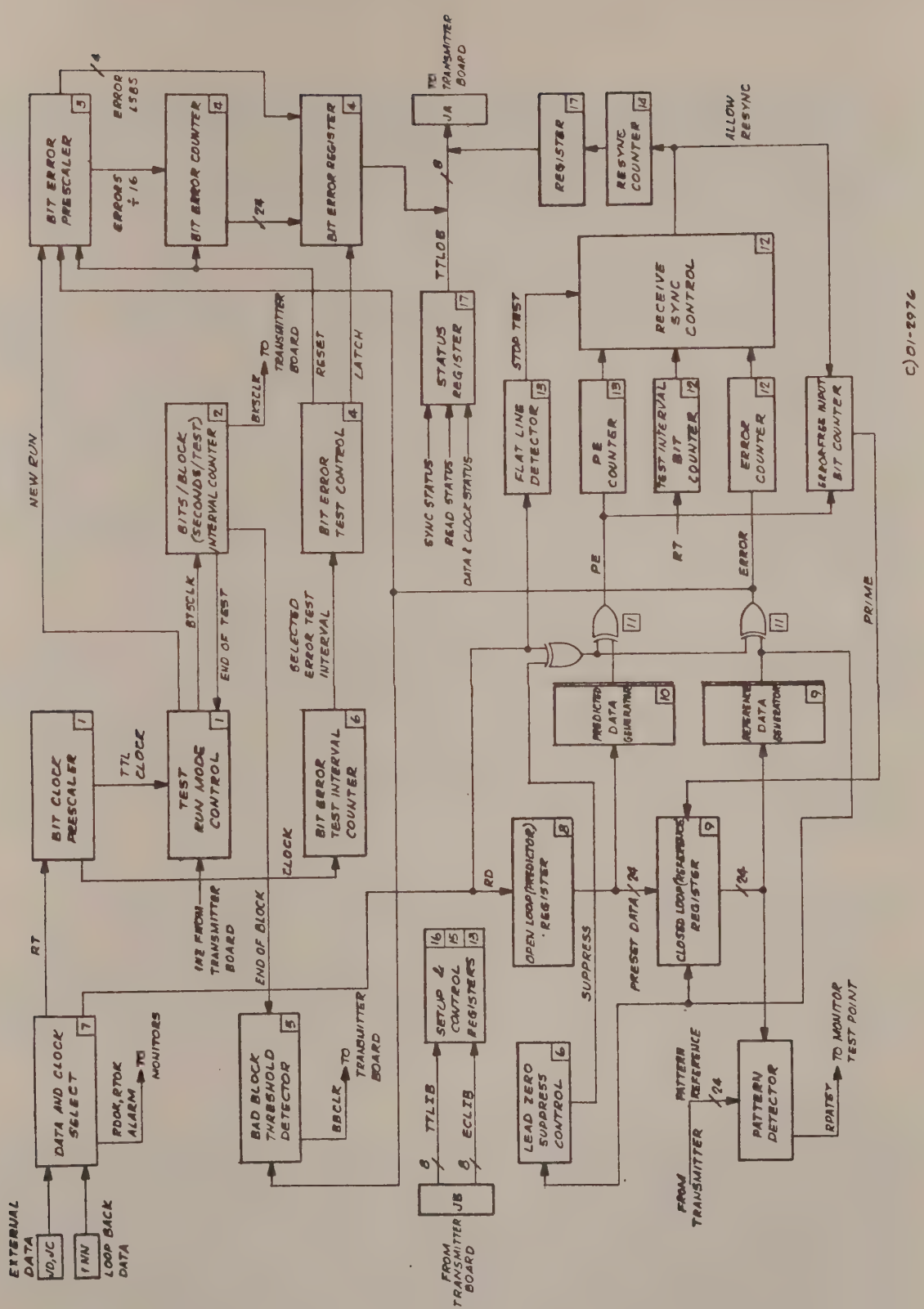


Figure 4-4. Receiver Board GP031-1, Detailed Block Diagram

The selected data and clock are input to the open loop register (OLR). A predicted data generator selects the appropriate taps on the OLR (per setup register) and outputs a bit, predicted to be the next input bit. By comparing this bit to the incoming data, Predictor Errors (PE) are derived. If PN patterns containing long strings of zeros are being utilized, the transmitting data source may be inverting the leading zeros to insure that no zero string contains more than 14 consecutive zeros. A lead zero supress circuit in the receiver predicts an early PN sequence, and, if it determines a string of 15 or more zeros are to be received, intitiates an inversion of the received data to compensate for the transmitter-inverted lead zeros. This function prevents false error bit decisions when compared to the predicted or reference data.

Received errors will be propagated through the OLR, thus genrating erroneous predicted data. Therefore, the OLR is useful in rapidly gaining information on the quality of the incoming data, but unsuitable for detecting exact bits in error counting. For this latter purpose, a second shift register is included, which is normally operated in a closed loop configuration; data predicted is fed back to the input of this shift register. Therefore, once an error-free-sequence of the pattern is placed in the closed loop register (CLR), error-free data will be generated, which can be used as a reference to compare the received data.

An error-free input bit counter constantly monitors the PE signal. Each detected error presets the counter to a value held in a setup register. The value equals twice the length of the longest tap used for predicting data. The counter insures that the OLR contains an error-free sequence of the pattern being transmitted. If the receive sync control logic determines the CLR is not synchronized with the incoming data, the error-free input bit counter generates a PRIME pulse when 2N error-free bits are received. The PRIME signal causes the parallel transfer of OLR data into the CLR during one bit time. Subsequently, the CLR is returned to closed loop operation, in synchronization with the incoming data.

Receiver synchronization is monitored by the receive sync control logic based on inputs from PE, test interval bit, and error counters and a flat line detector. Synchronization tests are run by the receive sync control logic and result in decisions to either initiate resynchronization, or halt the sync test due to a high PE or a low error rate.

The receive sync control inhibits a sync test from occurring until a data bit error is detected. Up to this time all counters and sense latches are reset or clamped. After an error occurs, the test interval bit counter begins to increment, enabling the PE and error counters. Various windows are set up by the test interval bit counter, which

monitors the PE and error counters to determine if the reference data generator is or is not in sync with the received data, and if the received data correlates with the expected pattern. The receive sync control is reset during a sync test if an out-of-sync condition is determined, if an in-sync condition is determined, or if the received data does not correlate with the predicted data. When reset, the receive sync control clears all counters and latches associated with the sync test until a new test is initiated.

The receive sync control is also reset or inhibited if a no transition or flat line condition is detected. When the OLR is set to recognize correlation of a pseudorandom sequence, it will also indicate correlation if the received data becomes all zeros. When the received data does not match the reference data generator, but correlation is indicated by the OLR, a resync normally occurs. The all zero input is detected however, by the flat line detector, thus inhibiting the receive sync control from conducting a sync test. The flat line detector is composed of a counter that is incremented by the receiver clock and reset by the output of a comparison gate monitoring the received data and the received data delayed by one bit time. Whenever these data signals are not the same, a reset to the counter occurs. If the received data is a constant one or zero, no reset is generated and the counter will issue a STOP command to the sync test circuits after 26 consecutive bit comparisons are detected. The flat line detector is inhibited when the all one data pattern, all zero data pattern, or recirculated pattern is selected.

The synchronization test, performed by the receive sync control logic, uses three counters to make a statistical determination of the sync status. The test interval bit counter records the number of elapsed bits from the beginning of a sync test period, and generates up to three test windows for pseudorandom data patterns. The significant counts occur at 128 bit times (SHORT test), 512 bit times (MEDIUM test), and 1536 bit times (LONG test). The sync test also uses the error counter which accumulates bit errors from the start of each sync test. Control gating senses a count of 48 errors, 192 errors, or 720 errors during a test. The PE counter, also used by the sync test, provides outputs for correlation counts of 32 and 720.

The Model 607 DTTS synchronization circuits are designed to synchronize and remain in sync with a high probability at error rates of 25 percent or even higher. Steady error rates of this magnitude would not normally be expected on a link, but since the Model 607 DTTS can be operated under such adverse conditions, tests are not easily disrupted by momentary bursts or dropouts. The dual register approach allows a high resistance to false resynchronization while maintaining a quick reaction time when synchronization is required. The reaction time is enhanced by the variable length of the sync test which requires longer tests only under adverse conditions.

The SHORT test allows a quick decision of the sync status at low error rates. The expected (mean) values for the bit errors and correlation (predictor) errors after 128 bit times are as follows:

Bit errors (in sync) at 0.10 error rate for 128 bits	= 12.8
Bit errors (in sync) at 0.25 error rate for 128 bits	= 32
Bit errors (out of sync) for 128 bits	= 64
Random data resultant errors for 128 bits	= 64
Correlation errors at 0.10 error rate for 128 bits	= 31.2

For the SHORT test, the following thresholds are used.

At 128 bit times:

If correlation errors $\geq$ 32, go to MEDIUM test.
If correlation errors $<$ 32, bit errors $<$ 48, STOP test.
If correlation errors $<$ 32, bit errors $\geq$ 48, allow a RESYNC.

Note that if the correlation (predictor) errors are below the nominal ten percent error rate value at the end of the SHORT test window, an in-sync or out-of-sync decision will be made and the sync test will be terminated. At error rates of four percent or better, the probability of a sync test running only 128 bits for an in-sync or out-of-sync determination is better than 99 percent.

The MEDIUM test includes the accumulated errors obtained during the SHORT test. During the 512 bit MEDIUM test, a decision is formulated based on the judgment of whether an out-of-sync condition may really exist (allow the LONG test) or if the errors were a result of burst errors or a high error rate. A GO/NO GO decision to continue the test is made and if there is sufficient doubt that a RESYNC is required, the test is terminated so that a new test can be initiated immediately.

The expected (mean) values for the MEDIUM test are as follows:

Bit errors (in sync) at 0.25 error rate for 512 bits	= 128
Bit errors (out-of-sync) for 512 bits	= 256
Random data resultant errors for 512 bits	= 256

For the MEDIUM test, the following thresholds are used.

At 512 bits:

If bit errors $<$ 192, STOP test.
If bit errors $\geq$ 192, continue into LONG test.

The LONG test makes use of the results accumulated during the SHORT and MEDIUM test and makes the final decision on whether an in-sync or out-of-sync condition exists. The 1536 bit time duration window allows an adequate amount of data to be accumulated for a positive decision at the higher error rates.

The expected (mean) values for the LONG test are as follows:

Bit errors (in sync) at 0.25 error rate for 1536 bits	= 384
Bit errors (out-of-sync) for 1536 bits	= 768
Random data resultant errors for 1536 bits	= 768
Correlation errors at 0.25 error rate for 1536 bits	= 672

For the LONG test the following thresholds are used.

At 1536 bit times:

If correlation errors $\geq$ 720, STOP test.
If correlation errors $<$ 720, bit errors $<$ 720, STOP test.
If correlation errors $<$ 720, bit errors $\geq$ 720, allow a RESYNC.

When the correlation error threshold of 720 is reached, the sync test is halted immediately, even if before 1536 bit times. The assumption is made that the data is corrupt and that a sync determination cannot be made. A momentary dropout or error burst will thus be recorded as errors and will not disrupt the operation of the test set by causing a false resync. When the correlation errors are less than 720, it is assumed that the correct pattern is being received and the sync status is then determined based on the bit errors.

The median value for bit errors for the in-sync and out-of-sync states is 576. Increasing the bit error threshold above this value gives the synchronization circuits a higher resistance to false resynchronization but increases the possibility of stopping a test instead of resyncing when an out-of-sync condition exists. A convenient threshold of 720 was used to give a maximum resistance to false resynchronizations while holding the probability of failing to recognize an out-of-sync condition during a sync test to less than one in a hundred tests at error rates approaching 25 percent. If a test fails to recognize an out-of-sync state, the next test will most probably recognize the condition as the probability of two successive failures is very high. Of course, at lower error rate, the probability of failure is greatly reduced.

When an out-of-sync state is recognized by a SHORT or LONG test, the resync logic is activated. This condition remains until the resync counter detects an error-free sequence of 2N bits and issues a resync pulse. When the resync logic is activated, the receive sync control is reset and clamped inactive, the sync status bit is negated, and all test functions (elapsed time and error counts) cease. When the 2N error-free sequence is recognized by the resync counter, the RESYNC indicator is latched ON, the reference data generator is primed with new data, the sync status bit is set, and all count and test functions are enabled. The RESYNC control remains on while the operator depresses the RESYNC key.

The synchronization test for the word mode uses a SHORT test window of 1024 bits and eliminates the MEDIUM test. Recognition of the sync status in the word mode is limited to lower error rates than when operating with pseudorandom patterns. For an out-of-sync condition with a pseudorandom pattern the bit error rate is nominally 50 percent. In the word mode, however, the out-of-sync error rate could be as low as 5% with a 20-bit word mismatching the reference data generator in only one bit position. If the error rate is 1% or better, the probability of making a sync status decision during a single sync test is better than 0.99. The Model 607 DTTS can hold sync and operate at high rates in the word mode, but a resynchronization, when necessary, requires more time.

To facilitate direct oscilloscope data link observations and measurements, a pattern detector is included on the receiver board. This circuit contains a comparator, which transitions when the CLR matches a selected reference pattern of the data. For PN data, this pulse, which is the Receive Pattern Sync (RPATSY) signal, occurs only once per PN sequence, and is useful for scope synchronization.

Two modes of tests are available with the Model 607 DTTS: continuous or interval. A continuous test is a freerunning accumulation of bit errors, blocks, block errors, seconds, and seconds errors; an interval test includes bit error rate and block/seconds throughput measurements. One set of counters are utilized exclusively for bit errors and bit error rate testing. Operation at rates up to 100 Mbps require the least significant 4 bits of error to be counted using ECL logic. A bit error prescaler accumulates the least significant digits of bit errors, and supplies an error rate, divided-by-16 signal to a 24-bit, TTL-based error counter. This counter is sized to facilitate 100% errors at 100 Mbps for a period of approximately 2½ seconds. During this time, the processor can sample the counter and accumulate the data, in floating point format. This approach yields a counter capable of totalizing 9.9×10^{99} bits in error (approximately 360 years at 100 Mbps) before overflowing.

Bit error rate is derived by counting bit errors over a fixed period of time. For example, 17 errors in 1 million bits corresponds to 1.7×10^{-5} BER. Logic circuitry for BER testing is provided on the receiver board. A bit error rate test interval counter contains decode counters and a multiplexer for selecting a base interval (10^2 through 10^9 bit times). The selected interval pulse is used by the bit error test control logic to transfer the error count to holding registers and resets the ECL and TTL bit error counters.

A second set of test counters are used to measure block/seconds related data. The test run mode control logic selects the clock source (per setup register) as either the bit clock or 1 hertz pulse. When

the run bit becomes set in the test run mode control register, the bit/seconds clock (BTSCLK) is gated ON and testing begins. A counter is preset with the bits per block (or seconds per test) and begins counting. Terminal count signifies the end of a block (or end of a test in seconds mode). The block/seconds clock (BKSCLK) output is counted on the transmitter board, where space was allocated for its TTL counter. The BKSCLK signal is also used by the bad block threshold detector. This circuit contains a bit error counter, whose count is compared against an allowable number (held in setup registers, 0-15) of errors. Each occurrence of the BKSCLK signal resets the counter. If the threshold was exceeded, a bad block/seconds clock (BBSCLK) will be output for counting on the transmitter board. The number of bad blocks and total blocks received is read by the processor board, and used to derive block/seconds throughput.

Control of the receiver board is accomplished via command bits and counter lengths loaded into setup registers. An eight bit TTL and eight bit ECL data input bus originates on the transmitter board. Register write strobes accompany the data bus and load the selected register, as decoded on the transmitter board. Bit error count, number of resync tries, and status are all readout on a TTLOB. Register output enable signals are decoded and sourced on the transmitter board.

4.3.4 INTERFACE BOARD

Interfaces to external communication circuits under test are operator selectable for a variety of interface specifications and protocols. All transmit interfaces can be active, regardless of the selected receive interface. Transmitter output signals are Send Data (SD) and Terminal Timing (TT). Other signals, Receive Data (RD), Receive Timing (RT), and the external transmitter clock input, Send Timing (ST) are selected by the operator as a group. The selected RT or RD interface also establishes the active ST input interface, regardless of the desired transmitter output interface.

Selection of the interfaces is provided on Page 2 of the CRT display. Upon entering the Run mode, the updated interface selection is passed from the processor board to the transmitter board, where it is decoded into discrete interface enable lines, and wired to the interface board. The interface board selects the active interface input through a multiplexer. Output from the multiplexer drives the receiver board's data receiver and error detection section.

4.4 SUBASSEMBLY CONFIGURATION

This section describes the four major subassemblies (PSR024-2; A2; GPO29-1, A5; GPO31-1, A6; and INF014-1, A1) of the Model 607 DTTS, referencing logic diagrams to aid in understanding the various functions. The other three subassemblies (CRT, A4; SM-160, A7; and FPK001-1, A8) are described in Appendices B, C, and D. Each of the major paragraph headings in this section lists the number of the corresponding logic diagram or schematic located in Section 6.

4.4.1 PROCESSOR BOARD (PSR024-2; Logic Diagram 500-0712, sheets 1-11)

The processor board is a microcomputer based on a Zilog Z80 microprocessor with the following peripheral logic:

- 14k bytes of PROM
- 4k bytes of RAM
- 1k bytes of non-volatile RAM
- Operator Keyboard interface.
- DMA/CRT display controller.
- HP Model 5150A printer interface (utilizes IEEE-488 bus).
- RS 232 printer interface (optional)
- 16-bit parallel interface to the ECL boards.
- 24-bit parallel frequency synthesizer interface.
- 4-bit parallel communications interface select control.

The processor board controls display of operating parameters and test results on the CRT monitor and controls the transfer of data between this display and the various device interfaces listed above.

4.4.1.1 Display Format. The CRT display is produced by intensity modulating the raster scan of a standard CCTV monitor operating in a non-interlaced repeat field mode. Character and display raster formats are shown in Figures 4-5 and 4-6. Fifteen character lines of 32 characters per line are displayed, with each character formed in a 7 column by 9 row dot matrix within a 10 column by 16 row character body. Each row of dots is displayed on a separate TV scan line. The 9 rows in the character matrix occupy rows 2 through 10 in the character body. Individual characters can be assigned any combination of underline, blink, and reverse video attributes. The underline is displayed on the 14th scan line. Reverse video is produced by inverting the normal white (unblanked) on black (blanked) display during the top 12 scan lines. Scan lines 13 through 16 are always normal display. Blink is produced by alternating the character with a space at a 2 Hz rate. The cursor is displayed as a blinking underline. The full 128-symbol ASCII character set is shown in Figure 4-7. All are available in the character generator, but only the characters in the four middle columns are utilized for the Model 607 DTTS display.

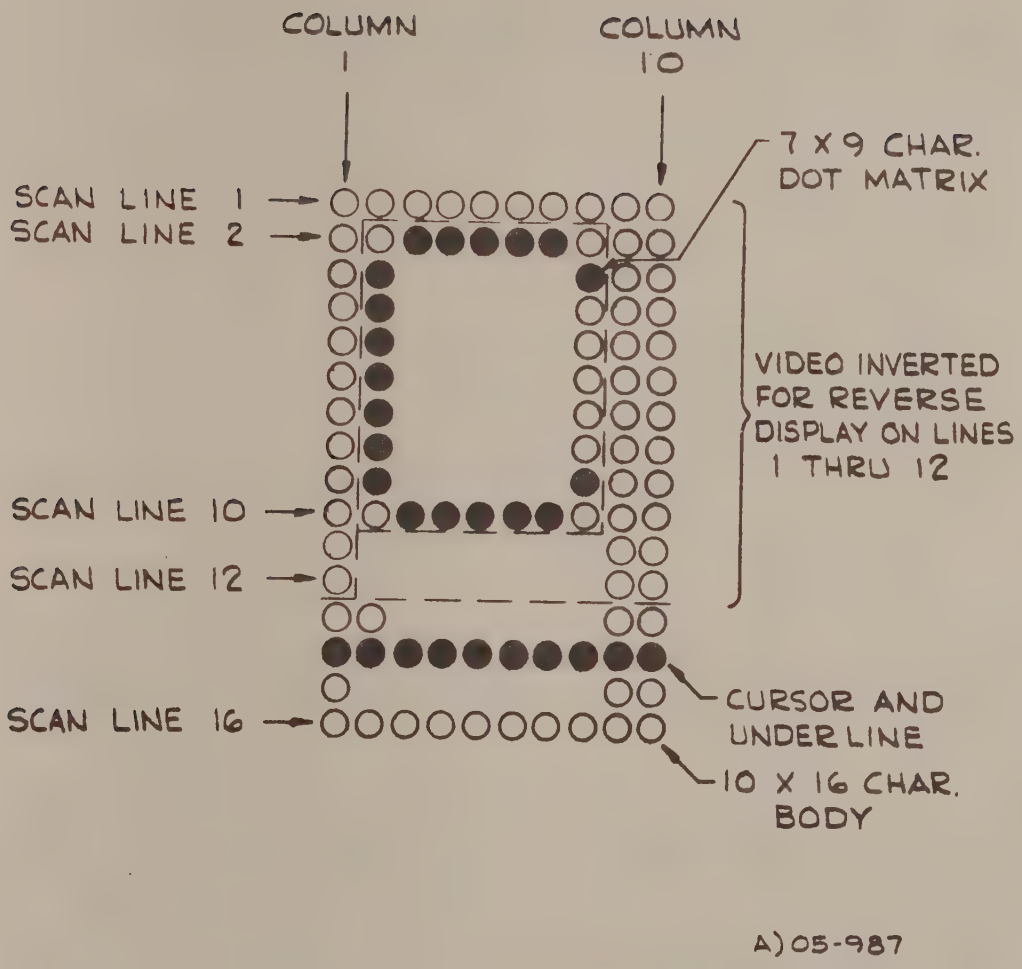
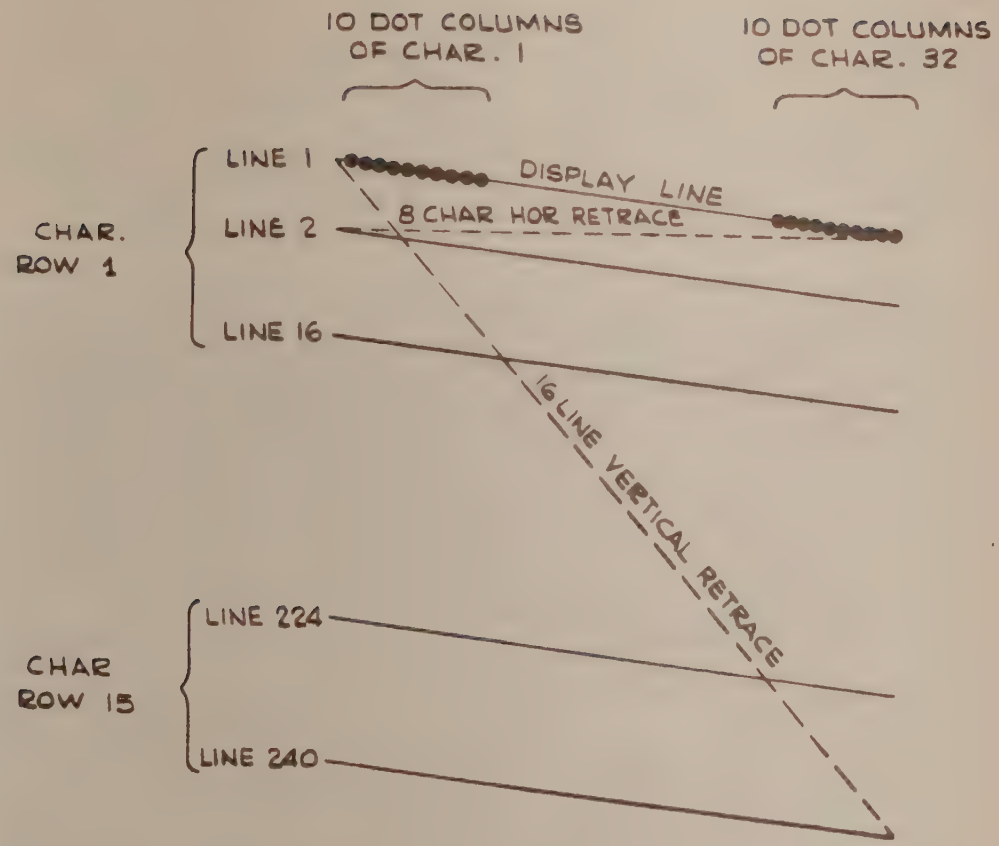


Figure 4-5. Character Format



HORIZONTAL REPETITION RATE:

= 6.144 MHZ DOT RATE/10 DOTS PER CHAR/40 CHARS PER LINE

= 15,360 KHZ

VERTICAL REPETITION RATE:

= 15,360 KHZ LINE RATE/256 LINES PER FRAME

= 60 HZ

A)05-986

Figure 4-6. CRT Display Raster

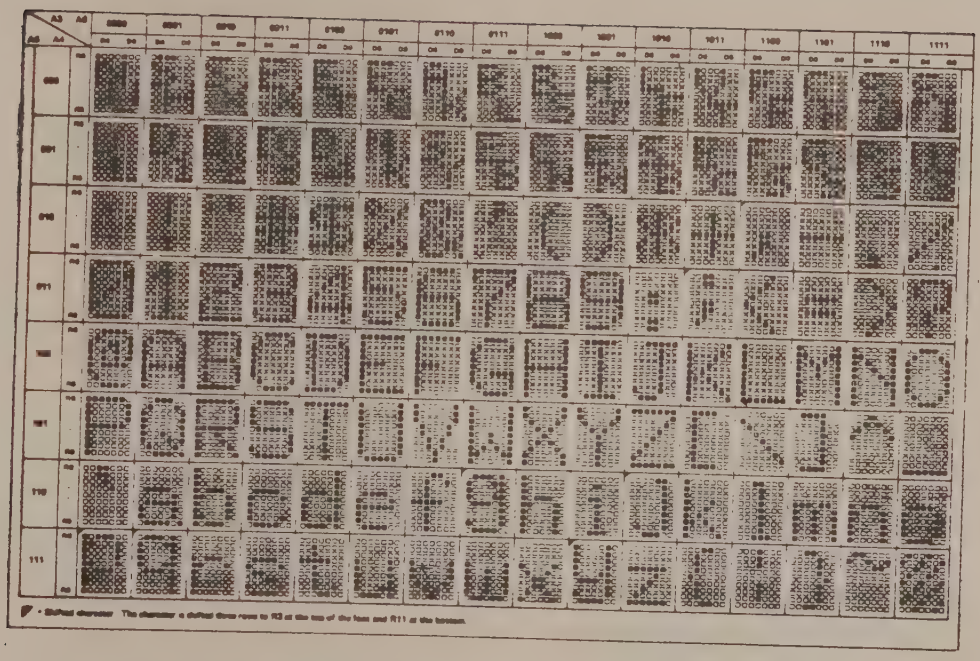


Figure 4-7. Model 607 DTTS ASCII Character Set

4.4.1.2 Memory and I/O Port Address Assignments. Memory and I/O port address assignments are shown in Tables 4-1 and 4-2.

Table 4-1

Memory Address Assignments

Address (Hex)	Function
0000 - 07FF	PROM DA39
0800 - 0FFF	DD39
1000 - 17FF	DG39
1800 - 1FFF	EA39
2000 - 27FF	ED39
2800 - 2FFF	EG39
3000 - 33FF	RAM BA42, BC42
3400 - 37FF	BE42, BG42
3800 - 3BFF	BJ42, CB42
3C00 - 3FFF	CD42, CF42 (Display Refresh)
4000 - 47FF	Unassigned
4800 - 4BFF	NON-VOLATILE RAM DE19
4C00 - 4FFF	Unassigned
5000 - 57FF	PROM FA39 (Not Implemented)
58FF - FFFF	Unassigned

Table 4-2

Port Address Assignments

Address (Hex)	Decode (Octal)	Device	
		Input	Output
00	000	PIO PORT A DATA	PIO PORT A DATA
01	001	PIO PORT A CONTROL	PIO PORT A CONTROL
02	002	PIO PORT B DATA	PIO PORT B DATA
03	003	PIO PORT B CONTROL	PIO PORT B CONTROL
04	004	SIO (RS 232) DATA	SIO (RS 232) DATA
05	005	SIO (RS 232) CONTROL	SIO (RS 232) CONTROL
06			
07			
08	010	8291 DATA IN	8291 DATA OUT
09	011	INT STATUS 1	INT MASK 1
0A	012	INT STATUS 2	INT MASK 2
0B	013	SER POLL ADD	SER POLL MODE
0C	014	ADDRESS STATUS	ADDRESS MODE
0D	015	COMM PASS THRU	AUX MODE
0E	016	ADDRESS 0	ADDRESS 0/1
0F	017	ADDRESS 1	EOS
10	020	8275 PARAMETERS	8275 PARAMETERS
11	021	CONTROL	CONTROL
12			
13			
14			
15			
16			
17			
18	030	KEYBOARD 1	
19	031	KEYBOARD 2	INTERFACE SELECT
1A	032	KEYBOARD 3	NVRAM MODE
1B	033	488 INT ADDRESS SWITCH	8275 DATA
1C	034	(Unassigned Switches, 4 LSB)	
1D	035		FREQ SYN MS DIGITS
1E	036		FREQ SYN 2nd MS DIGITS
1F	037		FREQ SYN LS DIGITS

Table 4-2. Port Address Assignments (cont.)

Address (Hex)	Decode (Octal)	Device Input	Output
20 21 22 23 24 25 26 27		Unassigned	Unassigned
28 29 2A 2B 2C 2D 2E 2F	050	DMA	DMA
30 31 32 33 34 35 36 37	060 061 062 063	CTC CNT 0 (Unassigned) CTC CNT 1 (1 Hz INT) CTC CNT 2 (60 Hz INT) CTC CNT 3 (Unassigned)	CTC CNT 0 CONTROL CTC CNT 1 CONTROL CTC CNT 2 CONTROL CTC CNT 3 CONTROL

4.4.1.3 Microprocessor. The Z80 microprocessor module AA10 and the associated bus and control signal interface logic, shown on sheet 1, are described below:

a. Data Bus. The 8-bit Z80 data bus, DBØ through DB7 is connected to peripheral devices through bi-directional, tri-state buffers AH10 and AH22. The RD (H) signal on AH10-15 and AH22-15 connects peripheral data to the processor during Read and Interrupt operations, and processor data to peripheral devices during Write operations. BUSACK (H) on AH10-1 and AH22-1 sets the buffer to a high impedance state during Direct Memory Access (DMA) operations.

b. Address Bus. The 16-bit Z80 address bus, ABØØ through AB15, is connected to peripheral devices through tri-state buffers AD10, AF10, and AD22. BUSACK (H) on pins 15 of these modules sets the address outputs to the high impedance state during DMA operations.

c. Output Control Signals. Processor output control signals are distributed to peripheral devices through buffers AF22 and AD22. During DMA operations BUSACK sets all output control signals to the high impedance state, except the signal BUSACK itself.

d. Input Control Signals. There are several different input control signals:

(1) One interrupt signal, INT at AA10-16, is described in paragraph 4.4.1.6.

(2) The WAIT input is utilized only by the non-volatile RAM described in paragraph 4.4.1.9.

(3) The Bus Request signal, BUSRQ at AA10-25, is utilized for DMA transfers by the display control logic described in paragraph 4.4.1.10.

(4) The RESET input at AA10-26 is set active momentarily when the equipment is energized and a RESET signal is generated by AC35-3.

4.4.1.4 Processor Board Timing. The microprocessor and video timing are derived from a single 18.432 MHz crystal oscillator AA44, shown on sheet 1. The TTL level square wave output of the oscillator is counted down 8 to 1 by synchronous binary counter AA34 to produce 2.3 MHz for the microprocessor and its peripheral modules. It is also supplied to sheet 6 to generate the video timing described in paragraph 4.4.1.10.

The 60Hz Vertical Blanking (VB) signal, generated by the display control logic, is counted down to 1 Hz by 4-bit binary counters CE25 and CG25 and flip-flop CE34-9 on sheet 3. The 1 SEC (L) output is used as a 1 Hz interrupt source for the CTC module at CE10-22 and, inverted by CG34-4, is supplied to the ECL logic through F-18 as the 1 SEC (H) signal.

4.4.1.5 Address Decoding. The address bus is decoded to provide enable signals for the memory and I/O devices. Address decoding is implemented by the logic on sheets 2 and 3.

a. Memory Addresses. Decoder modules AC43 and AE43 on sheet 2 are enabled when memory is addressed by the MRQ signal on sheet 1.

(1) PROM Addresses. Signals, ROM A ENA, ROM B ENA, ROM C ENA, and ROM D ENA on sheet 2, each select 4K bytes of PROM. Signals ROM DCD 1 at AC35-06 and ROM DCD 2 at AC35-11 complete the decodes to select individual PROM modules. Detailed PROM address assignments are described in paragraph 4.4.1.7.

(2) RAM Addresses. On sheet 2, the signal from AC43-12 selects RAM memory addresses 3000H through 3FFFH, and enables AE43-12 through AE43-9 to activate individual RAM modules. Detailed RAM address assignments are described in paragraph 4.4.1.8.

(3) Non-Volatile RAM Addresses. The signal from AC43-11 selects NVRAM memory at AE43-6 (addresses 4800 through 4BFF), enabling signal NVRAM ENA (L) to activate NVRAM module DE19 on sheet 9. AE43-4, AE43-5 (addresses 4000 through 47FF) and AE43-7 (addresses 4C00 through 4FFF) are unassigned.

b. I/O Device Addresses. Decoder module CG01 and DC13 on sheet 2 are enabled when an I/O port is addressed by signal IORQ at DE10-1. Module DC13 outputs select groups of eight ports, both input and output. Module CG01 completes the decode of input ports and DG10, on sheet 3, completes the decode of output ports.

c. Decode Mnemonics. Many memory and I/O port address decoders have mnemonics which are descriptive of the octal addresses which enable them. For example, at DG10-15 on sheet 3, OUT PORT 030 is enabled by a Write operation to PORT 00 011 000. This is a partial decode, with the eight most significant bits of the address bus not decoded and assumed to be zero. Other signals which provide only a partial decode of the eight least significant bits of the address bus have mnemonics of the form PORT 00X, which is active for addresses octal 000 through octal 007.

4.4.1.6 Interrupt Operation. The microprocessor is programmed to operate in the vectored Interrupt mode, in which any one of several peripheral devices may activate a common tri-state Interrupt line (INT) at AA10-16 on sheet 1. The interrupting device then places an identifying vector on the data bus in response to an interrupt acknowledge.

Priority of interrupts is determined by serially connecting Interrupt Enable (IE) lines between the devices in order of descending priority. The processor logic is wired to permit interrupts, which are generated by three devices with the following order of priority:

a. The PIO module, EC10 on sheet 7, has the highest priority. Its INT ENABLE input at EC10-24 is always high.

b. The DMA Controller module, BA10 on sheet 6, is enabled by a PIO IEO signal, and has second priority.

c. The CTC module, CE10 on sheet 3, which is utilized to insert 60 Hz and 1 Hz interrupts into the system, is enabled by a DMA IEO and has lowest priority.

The PIO and DMA controller modules are not programmed to generate interrupts, so the CTC module is always enabled, and is the only source of maskable interrupts. The following functions are performed by the CTC module:

a. CTC Addressing. The CTC module is enabled for programming by partial port decoder PORT 06X at CE10-16 on sheet 3. Registers within the module are selected by the two least significant bits of the address bus ABØØ and ABØ1, while addressing this port.

b. CTC Interrupts. The CTC module contains 4 counters, each of which may be programmed to generate an interrupt when counted down to zero. During turn-on initialization:

(1) Counters 0 and 3 are disabled.

(2) Counters 1 and 2 are enabled and loaded with a starting count of binary 01. This results in the generation of an interrupt for every positive transition of the input clock to each of these counters.

(3) Counters 1 and 2 are assigned unique vector addresses which identify their interrupts.

c. 1 Hz Interrupt. The counter 1 clock at CE10-22 on sheet 3 is connected to a 1 Hz square wave signal 1 SEC at CE34-9. When this signal occurs, the resulting INT signal at CE10-12 causes the microprocessor to call the routines which update the time display.

d. 60 Hz Interrupt. The counter 2 clock at CE10-21 on sheet 3 is connected to the 60 Hz VB signal at BH33-10 on sheet 6. When this signal occurs, the resulting INT signal at CE10-12 on sheet 3 causes the microprocessor to call the Keyboard and ECL interface update routines.

4.4.1.7 PROM. Sheet 4 of the logic diagram shows the PROM logics; 14,336 bytes of PROM are implemented with seven 2K x 8-bit 2716 modules. PROM is assigned addresses 0000 through 2FFF and 5000 through 57FF, listed in table 4-3.

Table 4-3

PROM Addresses

PROM Address (Hex)	Enable Signal	PROM
0000 - 07FF	ROM A ENA . ROM DCD1	DA39
0800 - 0FFF	ROM A ENA . ROM DCD2	DD39
1000 - 17FF	ROM B ENA . ROM DCD1	DG39
1800 - 1FFF	ROM B ENA . ROM DCD2	EA39
2000 - 27FF	ROM C ENA . ROM DCD1	ED39
2800 - 2FFF	ROM C ENA . ROM DCD2	EG39
5000 - 57FF	ROM D ENA . ROM DCD1	FA39

The 2716 PROM modules on sheet 4 are enabled when both pins 18 and 20 are set low by the listed enable signals from AC43 and AC35 on sheet 2. The 2048 bytes in each module are addressed directly by the 11 least significant bits of the address bus.

4.4.1.8 RAM. Sheet 5 of the logic diagram shows the RAM logics. 4K bytes of static RAM are implemented with the eight 1K x 4-bit 2114 modules. RAM is assigned addresses 3000 through 3FFF, listed in Table 4-4.

Table 4-4

RAM Addresses

RAM Address (Hex)	Enable Signal	Bits 0-3	Bits 4-7
3000 - 33FF	RAM A ENA	BA42	BC42
3400 - 37FF	RAM B ENA	BE42	BG42
3800 - 3BFF	RAM C ENA	BJ42	CB42
3C00 - 3FFF	RAM D ENA	CD42	CF42

The RAM modules are enabled when the signals listed above set pin 8 low. The four data lines (pins 11 through 14) of each 2114 module share read/write functions. If WRITE at pin 10 is active low when the chip is enabled, the data bus is stored in the 2114. If WRITE is inactive, the data stored in the 2114 is gated to the data bus.

4.4.1.9 Non-Volatile RAM. Non-volatile RAM is used to store the operating test conditions at each transition into the Run mode and to initialize the display with these conditions when the equipment is energized. 1K 4-bit bytes of Non-Volatile Random Access Memory (NVRAM) are implemented with the ER3400 module at DE19 on sheet 9. The NVRAM is assigned addresses 4800 through 4BFF, which are decoded as NVRAM ENA at DE19-15. The NVRAM operates in 4 modes, selected by a 2-bit code on inputs CØ at DE19-7 and C1 at DE19-8, listed in Table 4-5.

Table 4-5

NVRAM Code Inputs

CØ	C1	Command
0	0	READ
1	0	WRITE
0	1	BLOCK ERASE (not used)
1	1	WORD ERASE

The operating mode is loaded into buffer register DA30 (address OUT PORT 032) by the microprocessor prior to NVRAM access. The NVRAM has an access time of approximately one microsecond, too slow for direct microprocessor access without a WAIT period. When NVRAM is addressed, NVRAM ENA sets flip-flop CE34-5 initiating a WAIT period. The WAIT signal enables binary counter CC32 which clears WAIT after four 2.3 MHz clock cycles.

Writing data into the NVRAM requires the following sequence of operations:

a. Word Erase mode is set in buffer DA30.

b. A WR instruction is addressed to NVRAM. The module is enabled by NVRAM ENA and WR sets DE19-14 low. The contents of the data bus are "don't care"; the addressed byte is set to all 1's by the NVRAM I.C.

c. A 20 millisecond wait is required for the module to complete the byte erase (not the WAIT signal).

d. Write mode is set in buffer DA30.

e. New data is written into the erased address.

f. A 2 millisecond wait is required for the module to complete the byte write operation (not the WAIT signal).

g. Read mode is set in buffer DA30.

h. Two dummy read operations, addressing the modified byte, must be performed to prevent damage to the module.

For the read operation of the NVRAM, the mode buffer DA30 is always set to Read mode when not in the process of writing new data. Addressing a READ instruction to NVRAM enables DE19 by setting NVRAM ENA low. Following the WAIT cycle, the microprocessor reads the NVRAM output: bits 0 through 3 are NVRAM data (DE19-10 through DE19-13); bits 4 through 7 are always logic high (DC22).

The NVRAM requires a -30 vdc bias on DE19-1 for data write and erase operations. This voltage is supplied by the module at DE31, which converts a -12 vdc input at DG31-2,5 to the -30 vdc output at DE31-4, 7. Logics DC31 and DG31 contain components supporting the module at DE31. NVRAM data retention depends upon the -30 vdc bias being removed first on power-down and being applied last on power-up. The -4.7 voltage is quick to drop due to the heavy ECL at power-down, which opens the relay DJ31, disconnecting -30 vdc from DE19. At power-up the 6.8 uf capacitor at EB31-3 limits the -30 vdc rise time when power is turned on.

4.4.1.10 Display Control Logic. The display control logic is shown on sheet 6 of the logic diagram. The display control logic consists of:

a. A Zilog Direct Memory Access (DMA) module, BA10, which controls transfer of data from RAM display refresh memory to the CRT controller module.

b. An Intel 8275 programmable CRT Controller module BD10 which contains a character line buffer, visual attribute feature control, and the timing control necessary to generate the horizontal drive and vertical drive signals used for CRT synchronization.

c. A Motorola MCM66750 Character Generator Read Only Memory (CGROM), BG10, which converts ASCII character code and scan line count information from the CRT controller to a dot pattern which forms a line segment of that character.

d. A video shift register, CA10, which converts the 7-bit parallel output of the CGROM to a serial bit stream for input to the CRT monitor.

e. Dot timing logic and visual attribute synchronization and control logic.

Each of these components, which make up the display control logic, is described in the following paragraphs.

a. DMA Controller. The DMA controller module BA10 transfers display refresh data from RAM to the CRT controller module without microprocessor intervention. The DMA controller has access to the full data and address busses and to all microprocessor control lines. It operates in the following manner:

(1) The CRT controller device BD10 sets the RDY (H) line at BA10-25 to request data.

(2) The DMA controller sets BUSRQ (L) at BA10-1 to request control of the data and address busses from the microprocessor.

(3) The microprocessor acknowledges the request by setting BUSACK at BA10-14, which sets tri-state bus drivers AH22, AH10, AD10, AF10, AD22, and AF22 on sheet 1, to the high impedance state and initiates DMA controller bus operation.

(4) The DMA controller reads the next 8 characters from a predefined display refresh RAM area and transfers these characters to the CRT controller. These transfers utilize the busses and control lines in exactly the same manner and sequence as the microprocessor.

(5) The DMA controller releases BUSRQ (L), terminating the DMA operation and returning bus control to the microprocessor.

The microprocessor accesses the DMA controller for turn-on initialization by addressing PORT 05X at BA10-16. The unit is programmed with the following operating parameters:

(1) RAM to User only mode.

(2) User is OUT PORT 033 (CRT controller).

(3) RAM display page start address is 3C00.

(4) The block transfer length is 480 bytes (15 lines of 32 characters per line).

(5) Continuous transfer (upon completion block automatically restarts).

(6) Transfer bursts of 8 characters while RDY is active.

When a keyboard page operation is performed, the start address of the display block is alternately set to 3C00 (Page 1) to 3E00 (Page 2).

b. CRT Controller. The CRT controller BD10 contains a character display line buffer, timing control logic to generate horizontal and vertical drive signals for CRT synchronization, and visual attribute control logic. The unit is programmed with display parameters during turn-on initialization and with cursor position information anytime the cursor moves. These various internal display parameter buffers are addressed as a specific sequence of data to PORT 02X at BD10-22, with ABØØ at BD10-21 selecting control or data mode.

Turn-on initialization defines:

(1) 32 displayable and 8 retrace characters per line.

(2) 15 displayable and 1 retrace character lines.

(3) 16 scan lines per character line.

(4) The cursor is a blinking underline at the 14th scan line.

(5) 8 characters transferred per DMA cycle.

The CRT controller, having been programmed to this display format, generates a series of DMA request signals, RDY at BD10-5, resulting in the transfer of a row of 32 characters from display memory via the DMA controller to the module's row buffers. The CRT controller is addressed as PORT 033 at BD10-6 for data transfer. This sequence of 32 7-bit character codes is held until the end of the last (16th) scan line of the current character row, and then is transferred to outputs CCØ at BD10-23 through CC6 at BD10-29 at the 614.4 kHz character clock (BD10-30) rate during each of the 16 scan lines forming the character row. All codes are presented during each scan line. These codes and the 4-bit scan line count, BD10-1 through BD10-4, are input to a character generator ROM, BG10, which outputs the appropriate video dot patterns to display the characters. While this line is being displayed the characters for the next line are obtained from the DMA controller.

The CRT controller generates two display synchronization signals: Vertical Drive, VD (H) at BD10-8 and Horizontal Drive, HD (H) at BD10-7. Display data is synchronized to these signals by an "end of screen" character F3H, which must always occur as the last character on the bottom line of the display. Horizontal drive is active during the

8-diameter horizontal retrace period. Single shot CC01 shortens horizontal drive to approximately 1 millisecond for input to the CRT monitor. Vertical drive is active during the 16th scan line vertical retrace period.

Display attribute codes may be inserted in refresh data to affect the visual characteristics of a field of characters from the character following the attribute code to the next encountered attribute code or end attribute code. Display attributes may be any combination of blink, reverse video, or underline. The reverse video function is partially implemented by gating outside the CRT controller. Reverse video characters are identified by an active RVV signal at BD10-36. The underline function is also partially implemented by external gating logic. Signal LTEN at BD10-37 is active during the programmed scan line at underlined character locations. The cursor is displayed by LTEN occuring at the 2 Hz blink rate. The blink function is implemented by activating the Video Suppression output, VSP at DD10-35, at approximately 2 Hz. The VSP output drives gating logic externally to the CRT controller to disable video display. It is active not only during blink fields, but also during attribute control characters (to force a space delay at their location) and during horizontal and vertical blanking.

c. Character Generator. The character generator BG10 is a Motorola MCM66750 ROM, which contains the complete 128 character ASCII set in a 7 x 9 dot matrix. It is addressed by a character code BG10-15 through BG10-4 and by a scan line count BG10-21 through BG10-24. The character generator output is 7 bits (D0 through D6) defining the 7 dots forming the addressed character row; D0 at BG10-17 is the left most (first out) dot. The character generator ROM outputs the top row of a character at scan line 00H while the unit requires this line to be a blanked character border. For this reason 4-bit adder BG23 adds FFH (effectively subtracting 1) to the CRT controller line counter, shifting the video output down to scan lines 2 through 10 (01H through 09H).

d. Video Timing. Video timing is controlled by a module-3 counter AG34, which counts down the 18.432 MHz basic oscillator AA44 to the 6.144 MHz display dot frequency, and by a module-10 counter AJ32, which counts the dot rate down to the 614.4 kHz display character frequency. There are three outputs from these counters: AG34-13 is a 6.144 MHz video clock; BH33-02 is a 614.4 kHz clock used to shift characters from the CRT controller BD10; and CA22-6 defines the last (10th) dot period in a character body row. The CRT display raster has the following time relationships:

(1) Video dot rate = 6.144 MHz

(2) Horizontal Character Rate = $\frac{6.144 \text{ MHz}}{10 \text{ dots per char.}}$ = 614.4 kHz

(3) Horizontal Line Rate = $\frac{614.4 \text{ kHz char. rate}}{40 \text{ chars. per line}}$ = 15,360 kHz

(4) Character row rate = $\frac{15,360 \text{ kHz line rate}}{16 \text{ lines per row}}$ = 960 kHz

(5) Vertical repetition rate = $\frac{960 \text{ kHz row rate}}{16 \text{ character rows}}$ = 60 Hz

e. Output Gating and CRT Interface. The character generator video dot pattern and the corresponding CRT controller visual attribute outputs are all being accessed while the previous character's video is being shifted to the CRT. At the trailing edge of the last (10th) dot of the preceeding character period, defined by CA22-6, all of these signals are sampled:

(1) The character generator output is loaded into video shift register CA10. The first bit out of this register (column 1 in the character body) is loaded with a logic zero (blank). The 7 CGROM output bits are loaded into the next 7 bits of the shift register.

(2) The Reverse Video (RVV), Video Suppression (VSP), Horizontal Drive (HD), and Vertical Drive (VD) signals from the CRT controller are loaded into 4-bit buffer register BB32.

(3) The LTEN CRT controller output is loaded into 4-bit buffer register BD32.

Display of this character proceeds during the next 10-bit period while the next character and its attributes are being read from the CGROM and CRT controller.

The video dot pattern is shifted from CA10 by the 6.144 MHz clock at CA10-7. This video signal is gated in the following manner:

(1) A logic zero on CC22-1 gates the video stream off if VSP is active.

(2) A logic one on CC10-2 inverts the video if RVV is active; CA22-3 enables this inversion only during the top 12 scan lines of the character body.

(3) A logic one at BH01-3 forces the video to all one's (a horizontal bar) during scan line 14 when LTEN is active.

(4) Gate CA33-6 inverts the video over the entire screen if a flashing screen effect is desired. The 2 Hz signal on CA33- enables this inversion at a 2 Hz rate. Blanking signals on CA33-4,5 prevent the inversion during display retrace.

(5) The 6.144 MHz clock at BH01-6 serrates the video horizontally, producing dots rather than a solid line. Vertical seration is automatic because vertical columns are formed by video on different scan lines.

Gate BH01-4 drives the TTL level video directly to the CRT monitor. The latched vertical drive signal at BB32-14 drives the one-shot CC01 and outputs directly to the CRT monitor as VB. The latched horizontal drive signal at BD32-14 is delayed two character periods through BD32 before it triggers CC01 to produce a 1 millisecond HD signal for the CRT monitor.

4.4.1.11 ECL Interface. The microprocessor interface to the ECL logic is implemented with Zilog Parallel I/O Interface Controller (PIO) module EC10 and associated logic shown on sheet 7. The PIO module is addressed by partial decode AB = 00X on EC10-4. Various registers within the module are selected by the two LSB of the address bus, ABØØ and ABØ1. The PIO controls two 8-bit parallel ports, A and B. It is programmed during turn-on initialization to operate in a bidirectional mode, in which each port has certain characteristics.

Port A operates in a bidirectional mode for data transfers to and from the ECL logic. It utilizes the following handshake signals:

a. The signal ARDY at EC10-18 indicates to the ECL logic that an output word is available on Port A.

b. The signal $\overline{\text{ASTB}}$ at EC10-16 indicates that the ECL is reading this data. Port A data is stable until the trailing edge of ASTB.

c. The signal BRDY at EC10-21 indicates that the PIO is waiting for data from the ECL logic.

d. The signal $\overline{\text{BSTB}}$ at EC10-17 is tested by the processor. However, the ECL logic assembly responds with data faster than the processor can test the BSTB input. Therefore, no BSTB is supplied by the ECL board, the processor software assumes data is always ready when requested.

The modules FB01 and FD01 on sheet 7 are quad bidirectional tri-state drivers. FB01-15 and FD01-15 are held high to read data from AØ through A7 at all times except when ECL is reading output data, then $\overline{\text{ASTB}}$ gates the PIO Port A output to AØ through A7.

Port B (BØ through B7) is always output to the ECL interface. It utilizes no handshake signals. Port B contains an address code which defines the particular data word being transferred to the ECL logic on Port A or requests transfer of a particular data word from the ECL logic on Port A. The following pages outline the ECL interface word formats for Ports A and B.

4.4.1.12 Printer Interface. The interface to the HP Model 5150A thermal printer (optional) is implemented with an Intel P8291 GPIB Talker/Listener module (DJ10) and four transceiver modules EA01, EC01, EE01, and EG01, also shown on sheet 7.

The DJ10 module interfaces the microprocessor to an IEEE Standard 488 bus. It is programmed during turn-on initialization to operate in a talk only mode with the printer. The microprocessor addresses the DJ10 module as PORT 01X at pin 8. The three LSB of the address bus, ABØØ through ABØ2, select one of the 8 read or 8 write registers in the DJ10 module. Output data is addressed to PORT 01X, the first internal write register (ABØØ through ABØ2 = 000). The module drives the 8 bidirectional data lines DI01 through DI08 (pins 28 through 35) and 8 control lines (pins 24 through 27 and 36 through 39) of the IEEE-488 interface through the four transceiver modules. Pin 12 of the transceiver modules is held high by strap EF10-3 to EF10-12 to select active pull-up outputs. Replacing this strap with EF10-3 to EF10-11 will select open collector outputs for other applications. DJ10-2 holds pins 1 and 7 of modules EA01 and EC01 high to select output data. Input data transfers are never required.

Each character code output to the printer requires the following sequence of operations:

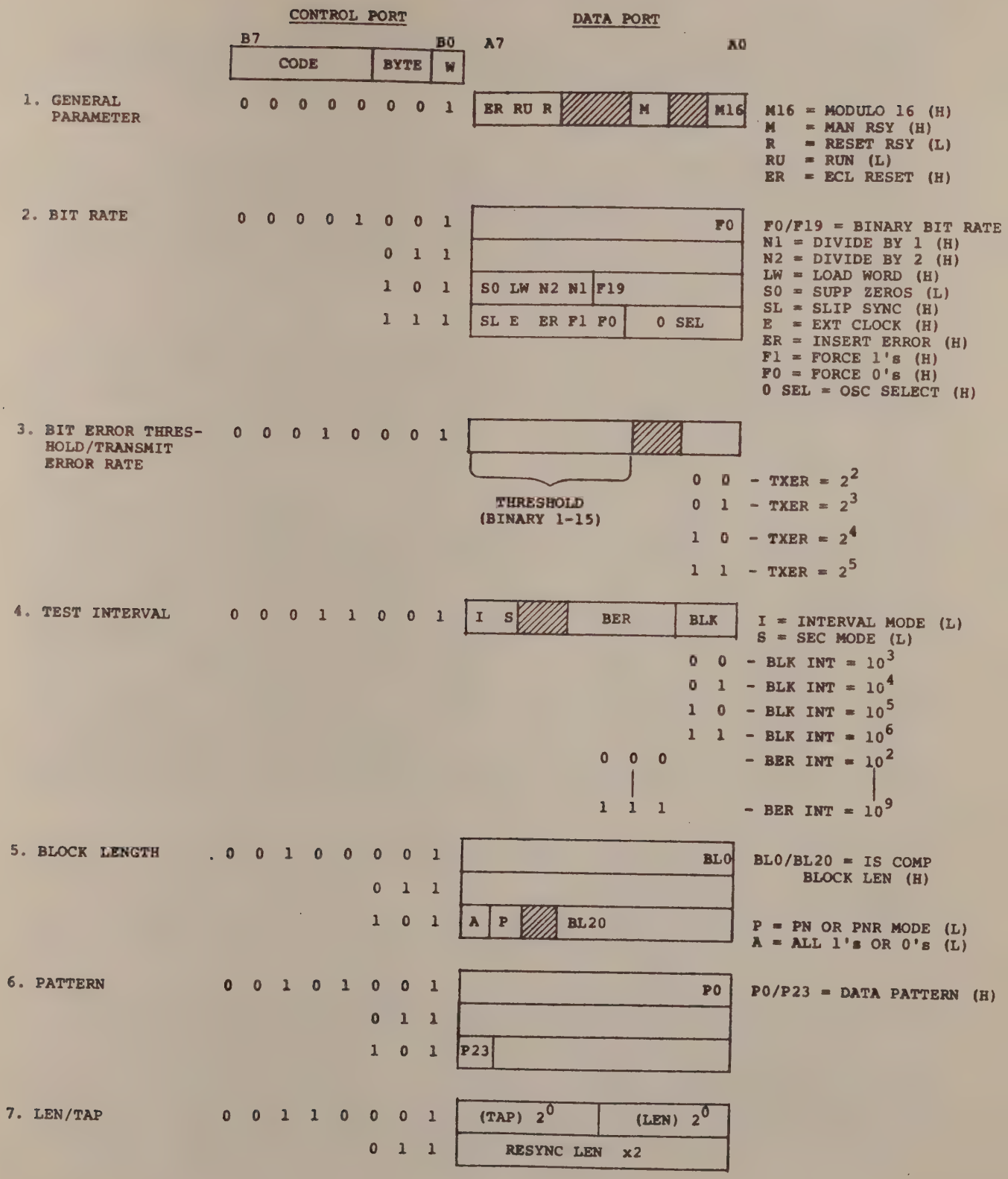
a. The microprocessor writes the character code into the DJ10 module output data register PORT 01X.

b. The DJ10 module gates the code to the output data lines and then sets Data Available (DAV) active low.

c. The printer reads the output data lines and then sets the NDAC line high.

d. The DJ10 module senses $\overline{\text{NDAC}}$, sets $\overline{\text{DAV}}$ inactive, and sets bit 1 in an internal interrupt status register.

ECL Interface Word Formats



CONTROL PORT

DATA PORT

		B7						B0	A7							A0	
		CODE					BYTE	W									
8.	MISCELLANEOUS	0	0	1	1	1	0	0	1	H	A	S	Z	TX	RD	RT	ST
9.	LATCH	0	1	0	0	0	0	0	1						L3	L2	L1
10.	READ BLOCK COUNTER	0	0	0	0	1	0	0	0	2^0							
							0	1	0								
							1	0	0	2^{23}							
11.	READ BLK THRUPUT	0	0	0	1	0	0	0	0	2^0							
							0	1	0								
							1	0	0	2^{23}							
12.	READ BER COUNTER	0	0	0	1	1	0	0	0	2^0							
							0	1	0								
							1	0	0								
							1	1	0	2^{27}							
13.	READ STATUS	0	0	1	0	0	0	0	0	BL	BE	BK	R	S	ST	RT	RD
14.	READ SYNC TRIES	0	0	1	0	1	0	0	0	MS DIGIT					LS DIGIT		

H = HIGH FREQ (H)
A = 50KA INT (H)
S = SEC MODE (L)
Z = ZERO SUPP (L)
TX= TX POL NOR (H)
RD= RD PRESENT (H)
RT= RT PRESENT (H)
ST= SELF TEST (H)

L1= LATCH BLKS (L)
L2= LATCH BLK ERRS (L)
L3= LATCH BIT ERRS (L)

BLOCK COUNTER (H)

BLOCK THRUPUT COUNTER (H)

BER COUNTER (H)

BL= BLOCK COUNTER RDY (H)
BE= BIT ERRORS RDY (H)
BK= BLK ERRORS RDY (H)
R = RESYNC (H)
S = SYNC (H)
ST= SEND CLOCK (H)
RT= RCV CLOCK (H)
RD= RCV DATA (H)

BCD SYNC TRIES (H)

e. After writing the character code into the GPlB module the microprocessor loops, reading the interrupt status register PORT 011. Upon sensing bit 1 active the microprocessor exits the loop and repeats this sequence for the next print character.

The HP Model 5150A printer interface parameters must be set as follows:

a. Carriage Return (CR) print character.

b. Addressable listener operation.

4.4.1.13 Keyboard Interface. The 20 front panel key switches provide operator control of the Model 607 DTTS operations. These switches are read directly by the microprocessor through tri-state drivers AG01, AJ01, BD01, and BF01 shown on sheet 8. The keys are Microswitch Series SD hall-effect switches mounted on a printed circuit board behind the front panel. Ribbon cables connect the switch outputs to processor board interface positions A and B, and also supply 5 vdc and ground from the processor board to bias the switches. The switches require output pull-up resistors AE01 and BB01. Switch output voltage is low active TTL compatible. Table 4-6 lists the switch interface modules for PORT 030, PORT 031, and PORT 032.

The microprocessor reads these three ports at a 60 Hz rate, updating the display or operating conditions as required. Switch bounce filtering is performed by the software and sampling rate. After any switch is depressed all other switches are locked out until all switches are released. The four cursor movement keys are unique in that their functions are repeated at a 2 Hz rate by the firmware, if they are depressed for more than one second.

4.4.1.14 Interface Select. The Model 607 DTTS interface is selected by the microprocessor through a 4-bit code output to buffer DA13 on sheet 8. The buffer is addressed as OUT PORT 031 DA13-11. Interface select codes are listed in Table 4-7.

Table 4-6

Switch Interface Modules

Signal	Bit	Input	Switch
PORT 030			
	0	AG01-2	Cursor Up
	1	AG01-4	Cursor Down
	2	AG01-6	Cursor Right
	3	AG01-10	Cursor Left
	4	AG01-12	Unassigned
	5	AG01-14	Unassigned
	6	AJ01-12	Unassigned
	7	AJ01-14	Unassigned
PORT 031			
	0	AJ01-2	Numeral 0
	1	AJ01-4	Numeral 1
	2	AJ01-6	Numeral 2
	3	AJ01-10	Numeral 3
	4	BD01-2	Numeral 4
	5	BD01-4	Numeral 5
	6	BD01-6	Numeral 6
	7	BD01-10	Numeral 7
PORT 032			
	0	BD01-12	ALT
	1	BD01-14	RESET
	2	BF01-2	HLT
	3	BF01-4	RUN
	4	BF01-6	PAGE
	5	BF01-10	Decimal Point
	6	BF01-12	Numeral 9
	7	BF01-14	Numeral 8

Table 4-7

Interface Select Codes

Code	Interface
0 0 0 0	TTL
0 1 0 0	BAL
1 1 0 0	BAL-BRG
0 0 1 0	50 KA
1 0 1 0	50 KA - BRG
0 1 1 0	T1
1 1 1 0	T1 - BRG
0 0 0 1	ECL
1 0 0 1	RS422

The interface select code is output to the ECL control board via connector C.

4.4.1.15 Frequency Synthesizer Interface. The frequency synthesizer is controlled by the microprocessor through a 6-digit BCD output stored in 8-bit buffer registers CH13, CJ01, and DB01 on sheet 10. The microprocessor addresses the two least significant digits at DB01 as OUT PORT 037 at DG10-7, the next two digits at CJ01 as OUT PORT 036 at DG10-9, and the two most significant digits at CH13 as OUT PORT 035 at DG10-10. Only one bit (100 MHz-1) of the most significant digit is utilized. The buffers are output to the frequency synthesizer through interface cables C and D.

4.4.1.16 Sequence of Firmware Operations. The processor board of the Model 607 DTTS is firmware controlled; the operating program is contained in 14K bytes of PROM. When the unit is energized, the microprocessor is automatically reset, which executes an initialization routine beginning at address 000H. This routine sets the operating modes of all programmable peripheral devices, clears and initializes RAM, and loads display refresh RAM with fixed field data from PROM tables and with the last entered variable field data from NVRAM. Following initialization the processor waits for interrupts. The 1 Hz interrupt causes the display time field to be updated by one second. The 60 Hz interrupt initiates the following operations:

a. A Key scan routine reads the front panel switch status and calls the appropriate key edit routines required to update the display.

b. A transition to Run mode causes the displayed test parameters to be output to the ECL logic.

c. The status of Keys which affect ECL operation is output to the ECL logic.

d. If in the Run mode, one of three display results is updated with data input from the ECL logic.

4.4.1.17 RS 232 Printer Interface. The RS 232 printer interface is implemented using a Zilog 84402PAOS SIO serial I/O controller (FF10), a 74LS393 counter (FF44), 1489 receivers (FD31), and 1488 drivers (FF31). These elements are shown on sheet 11 of logic diagram 500-0712.

The FF10 module interfaces the microprocessor to a standard RS 232 bus configured as the bus originator only via channel A (channel B is not used). The processor addresses port $00X_8$, where $X=4_8$ addresses the channel A data register and where $X=5_8$ addresses the channel A control register. The 74LS393 (FF44) divides the system clock by 4 and inputs it to the SIO for the serial and parallel converters. Handshake I/O and data output is routed through receivers at FD31 and drivers at FF31, which comply with RS 232 signal characteristic requirements.

Print operations require special interrupt handling because of 15 seconds needed for completion. Interrupts are enabled while a print is in operation, allowing 1 Hz time display update and 60 Hz results processing. The keyboard, however, is locked out, and the display, aside from the time field, is frozen at the start of print conditions.

4.4.2 TRANSMITTER BOARD (GPO29-1; Logic Diagram 500-0730, sheets 1-16)

The function of the transmitter board is to generate transmit timing and data. Transmit timing is generated via the transmit timing logic; transmit data is generated via the transmitter data logic and the error insertion logic. The following paragraphs describe the logics of the transmitter board. All logic modules referred to in this section are located on the transmitter board, unless otherwise noted.

4.4.2.1 Transmit Timing Logic. The function of the transmit timing logic is to generate and/or select the transmit timing clock, TT. Sheets 1 and 2 consist of the logic required to form the internal clock.

On sheet 1, the selection for the internal clock of either the synthesizer clock directly or a frequency of F/2N is provided by gate 7L-4. This selection is controlled by OR/NOR gate 3J-9, which senses the state 5 of the three select oscillator inputs S0Ø, S01, and S02. If the gate senses the state 5, the synthesizer clock is selected directly; for all other states, F/2N is selected.

On sheet 2, the frequency of F/2N is generated using a programmable binary down counter; a 3-input multiplexer, and a divide-by-two toggle flip-flop. The toggle flip-flop module 7M-4 insures a 50% duty cycle regardless of N. Input to this flip-flop is controlled by a 3-input multiplexer gate 7L-11. This multiplexer selects one of the three inputs F/N, F/2, or F under control of the two input signals N=1 and N=2. For N=1, the counter clock F is selected directly; for N=2, the divide-by-two counter clock F/2 is selected. For all other values of N, the programmable counter output F/N is selected.

The clock input to the programmable counter F is the selected output of a 16-input multiplexer module 7J. Select oscillator signals S0Ø, S01 and S02 are used to select any one of inputs I1 through I5. Input I5 is the frequency synthesizer. Inputs I1 - I4 can be preceded by modules 8FF and 7K, which together provide TTL to ECL conversion. The Model 607 DTTS is capable of operation with up to four crystal oscillator sources in addition to the frequency synthesizer input clock.

The programmable counter is designed to operate for values of N ranging from 4 to 2^{20}-1. The actual count is determined by the twenty binary input signals SFØ through SF19, which are applied to the parallel inputs of the five binary counter modules 6N, 6M, 6L, 6K, and 6J. When first operating, counter states 3 and 2 are sensed as a negative level using OR/NOR gates 7N. The signal is clock successively into D-type flip-flops 7M-11 and 7M-8. The output of these flip-flops occurs at a rate of F/N where N is the binary number represented by a 20-bit binary input. The Q output of flip-flop 7M-11 is used as a synchronous load input signal to the five counter modules. Since this load signal is two clock periods wide, the counter is actually synchronously loaded twice with the input value N. The count sequence is, therefore, 5, 4, 3, 2, N, N, N-1, etc. This technique is required in order to insure that the counter will operate at its maximum clock frequency for all values of N. More specifically, this technique allows two full clock periods for the terminal count of module 6M to ripple away at the output of module 6J, which is necessary for certain values of N at the highest clock rates.

On sheet 6, the final selection of internal or external clock is made via a 2-input multiplexer, gate 7L8. The multiplexer is controlled by the input signal EXTTT.

4.4.2.2 Block Counter and Interval Select Logic. The block counter and interval select logic are included on sheet 3. Since the input clock, BKSCLK, originates on the receiver board, module 5E is used as a line receiver and buffer. The block counter is a six-decade synchronous counter consisting of modules 6E, 6D, 6C, 6B, 6A, and 6X. The counter is cleared prior to each test by the MRT signal. The 24 counter outputs are applied as inputs to three, D-type, octal tri-state latches modules 7C, 7B, and 7A. These latches are loaded after every clock pulse as long as control signal $\overline{L1}$ remains in a high level state. When $\overline{L1}$ goes to a low state, subsequent clocks to the latches are inhibited and the latches retain the last transferred count. The outputs of the three latches are connected to the TTL Output Bus (TTLOB). Signals $\overline{R1A}$, $\overline{R1B}$, and $\overline{R1C}$ are used to enable the outputs of these tri-state latches, placing their contents on the bus.

Sheet 3 also includes the block interval logic. The purpose of this logic is to provide an output signal for each block interval when in the interval test mode, as controlled by the input signal CNTEST. The block interval is controlled by input signals SBIØ, SBI1, and SBI2. Table 4-8 gives the relationship between these signals and the actual interval.

Table 4-8

Input Signals/Blocks Per Interval

Input Signals			Block Per Intervals
SBIØ	SBI1	SBI2	
0	0	0	10^3
0	0	1	10^1
0	1	0	10^5
1	0	0	10^4
1	1	0	10^6

The actual output signal $\overline{\text{BLINT}}$, when it occurs, is a negative signal with a duration of one block.

4.4.2.3 Bad Block Counter and Rate Logic. The bad block counter and bad block rate logic are shown on sheet 4. The bad block counter is an 8-stage binary counter consisting of 4-bit binary counter modules 11E, 11D, 11C, 11B, 11A, and 11X. The clock input, BBSCLK, is generated by the bad block threshold logic. The 24 counter outputs are applied as inputs to the three tri-state, octal registers 10C, 10B, and 10A. The outputs of these three registers are connected to the TTLOB. The counter is cleared either by the $\overline{\text{MRT}}$ signal or at the end of each test interval.

When in the interval mode, the $\overline{\text{BLINT}}$ signal, which is negative for the duration of the last block in the test interval, is applied as the data input to 8-bit shift register 8X. The register is clocked by the BTSCLK. The QB and $\overline{\text{QC}}$ register outputs are combined at NAND gate 12A-8 to form a one-clock-wide negative pulse which is routed through 12A to the clock input of flip-flop 12B-3 as a positive pulse. The positive transition signals a positive pulse at 12B-6 and places the counter contents into the three registers 10C, 10B, and 10A. The $\overline{\text{QC}}$ and QD outputs of register 8X are combined in NOR gate 8A-4 to form a one-clock-wide positive pulse, which is inverted by 8A to clear the counter.

When in the continous mode, the CNTEST signal is high. The counter clock, BBSCLK, passes through module 12A to appear at the clock input to flip-flop 12B-3. The $\overline{\text{Q}}$ output of 12B-6 therefore, appears as an inverted, retimed version of input signal $\overline{\text{L2}}$. When $\overline{\text{L2}}$ goes low, 12B-6 goes high after the next positive clock transition. This posi-

tive transition at 12B-6 transfers the contents of the counter into modules 10C, 10B, and 10A.

4.4.2.4 Error Insertion Logic. The error insertion logic is illustrated on sheet 5 of the logic diagrams. The logic consists of a five-decade counter followed by a multiplexer. The counter consists of a one-decade prescaler module 3H connected as a decimal down counter. The prescaler output Q2 is converted to TTL form by ECL/TTL converter module 2FF-4. The TTL level signal is applied as clock to a four-stage, synchronous, decimal TTL counter consisting of modules 9E, 9D, 9C, and 9B respectively. The terminal count outputs of the final three decades are applied to an 8-input multiplexer module 8E. The multiplexer is controlled by three I/O signals, ADDERR, ER0, and ER1. Table 4-9 lists the error rate as a functions of these three input signals.

Table 4-9

Forced Error Rate Selection

Control Inputs			Forced Error Rate
ADDERR	ER1	ERØ	Errors/Bit
1	0	0	10^{-2}
1	0	1	10^{-3}
1	1	0	10^{-4}
1	1	1	10^{-5}
0	X	X	0

4.4.2.5 The Asynchronous 50 kb Clock Generator Logic. On sheet 6 of the logic diagram the asynchronous 50 kb clock generator logic is diagrammed. Binary counter modules 1D and 1E are clocked at a 5.6 MHz rate. When terminal count is reached, the counters are synchronously loaded to state 8 + 64 + 128 = 200. Since the terminal state is 255, the 5.6 MHz clock is divided by 56 to a rate of 100 kHz. The negative transition at the Q1 output of counter module 1D, which occurs when the counter is loaded, is used to toggle flip-flop 1B, forming the 50 kb clock. The input signal A50DAT is data received from the receiver board. This incoming data is clocked successively into D-type flip-flops 1C (pins 2 and 12 respectively). Their outputs are combined, using AND/OR gate 1A, so that after each data transition a positive pulse of one clock period in duration occurs. The pulse is used to control the phase or frequency of the counter signal which is used to synchronously load the counter. The pulse is also applied to pin 2 of D-type flip-flop 1B, which delays the pulse by one bit. The $\overline{Q}$ output is then applied to the preset input (pin 10) of flip-flop

1B, thus controlling the phase of the 50 kb clock. This technique insures that positive transitions of the internally generated 50 kb clock coincide with the incoming data transitions.

4.4.2.6 Transmitter Signal Monitors. Table 4-10 lists the selected monitoring transmitter signals. Each of these output signals is buffered using a 50 ohms, TTL line driver. These buffered signals are connected to pins at location 5X.

Table 4-10

Transmitter Monitoring Signals

Signal Name	Buffer Driver	Output Location	Logic Sheet
SPATSY	4E	5X-8	9
STMON	10E	5X-3	6
TTMON	10E	5X-4	6
SDMON	4E	5X-2	9

The SPATSY logic is shown on sheet 9 of the logic diagrams. Correlator modules 2N, 2M, and 2L each compare eight of the twenty-four data pattern inputs with eight of the twenty-four corresponding generator shift register output bits. A simultaneous A=B comparison for the three correlators occurs only once per transmitted pattern. The correlator outputs are combined in OR gate 3J-11 and the output is retimed using D-type flip-flop 1K-4. The output of this flip-flop is applied to flip-flop 2J-4, which is connected as a toggle flip-flop. Thus, the SPATSY monitor signal is a 50% duty cycle signal with a period equal to the time required to transmit two patterns.

The TTMON and SDMON signals monitor the transmitted timing and data respectively. The STMON signal also monitors the external sample clock. This clock is connected to the trigger input of flip-flop 4J-4, which is set by the 1 Hz HZ1ECL signal. When the external clock is present, the output of the flip-flop is high only when HZ1ECL is high. When the external sample clock is inactive, indicating no ST CLK present, 4J-4 remains high. The output 4J-4 is converted to TTL level by 7FF and applied to the D input of flip-flop 10D-2, clocked by a 1 Hz signal. The output signal of flip-flop 10D-5, STOK, is high when the external sample clock is active, and low when the clock is inactive. The STOK signal is routed via connector JA-9 to the receiver board, where it is input to register 5E-7. The outputs of this status register are monitored by the processor board.

4.4.2.7 Transmit Data Logic. The transmit data logic is shown on sheets 7, 8, and 9. The function of this logic is to generate the transmit data. Operation of this logic is described in the following paragraphs.

The transmitter data is generated via the transmitter pattern generator shown on sheets 7 and 8. The generator consists of a 24-bit shift register modules 3N, 3M, and 3L, length and tap multiplexers modules 1L and 1M, and EXCLUSIVE-OR gate 2K-13. Two types of patterns may be generated: recirculating and pseudorandom (PR). Recirculating patterns are formed by selecting a single input to gate 2K-13 from either the length or tap multiplexer. The output of 2K-13, SERIAL DATA, is fed back to the shift register input 3N-1. Therefore, whatever pattern of ones and zeros is in the shift register is recirculated, as selected by the multiplexers 1M and 1L. PR data is generated by the EXCLUSIVE-OR gate of two selected taps. SERIAL DATA input is again fed back to the shift register input, which generates a pseudorandom sequence of ones and zeros. This sequence repeats itself only once every 2^{N-1} bits, where N is the longest tap element. For example, a selection of the ninth and fifth taps results in a pattern 2^{9-1}, or 511 bits long. In the recirculate mode, selecting tap nine results in a 9-bit pattern. The actual selections are made via 4 select length inputs, SLØ-SL3, and 4 select tap inputs, STØ-ST3. Tables 4-11 and 4-12 list the shift register length inputs and shift register tap inputs, respectively. The unit is designed to operate for PR lengths of N=9, 11, 15, 20 and 23. For these patterns, the normal taps are for N=5, 14, 17, and 18 bits respectively. Taps required to reverse the sequence, N=2, 1, 3, and 5 bits respectively, are also available.

Sheet 7 of the logic diagram also shows the load word logic used for generating transmit data. Each time a new data pattern is selected for transmission, all 24 shift register stages must be loaded with a starting value. This value is stored in a 24-bit shift register consisting of modules 4N, 4M, and 4L. When a load word (LDWD) command is received from the I/O section, flip-flop 1K-11 is set to a high state. The next transmit timing clock transfers the signal to flip-flop 1K-8, which clears 1K-11, returning it to a low state. The next transmit timing clock returns flip-flop 1K-8 to a low state. A one-bit-wide load pulse is thus generated for each positive transition of the incoming LDWD signal. The one-bit-wide pulse synchronously loads the 24-bit shift register with the starting value.

Table 4-11

Shift Register Length Inputs

SL3	SL2	SL1	SLØ	Selected Length in Bits*	Function
0	0	0	0	-	Used for recirculating patterns.
0	0	0	1	-	
0	0	1	0	2	Used for dot pattern.
0	0	1	1	4	
0	1	0	0	6	
0	1	0	1	8	
0	1	1	0	10	
0	1	1	1	12	
1	0	0	0	13	
1	0	0	1	-	
1	0	1	0	9	
1	0	1	1	11	
1	1	0	0	15	
1	1	0	1	20	
1	1	1	0	23	
1	1	1	1	24	Used for ones pattern.

* Lengths not available in Table 4-11 (1, 3, 5, 7, 14, 16, 17, 18, 19, 21, and 22) are selectable via the tap multiplexer, as listed in Table 4-12. Therefore any bit length from 1-24 is possible for a recirculating pattern.

Table 4-12

Shift Register Tap Inputs

ST3	ST2	ST1	STØ	Selected Tap (M Bits)	Function
0	0	0	0	-	Used for recirculating patterns.
0	0	0	1	7	
0	0	1	0	16	
0	0	1	1	19	
0	1	0	0	21	
0	1	0	1	22	
0	1	1	0	4	Used for reverse normal pattern.
0	1	1	1	5	Pattern Length M=9.
1	0	0	0	2	Used for reverse normal pattern.
1	0	0	1	9	Pattern Length M=11.
1	0	1	0	1	Used for reverse normal pattern.
1	0	1	1	14	Pattern Length M=15.
1	1	0	0	3	Used for reverse normal pattern.
1	1	0	1	17	Pattern Length M=20.
1	1	1	0	5	Used for reverse normal pattern.
1	1	1	1	18	Pattern Length M=23.

Slip clock logic is shown on sheet 8 of the logic diagram. The function of the slip clock logic is to delete a single clock pulse to the transmitter pattern generator, which delays the pattern by a single bit, and causes the receiver, which will not have a clock deleted, to experience a loss of bit count integrity. Operation of the slip clock logic begins when the slip input switches from a low to a high state. The following clock pulse places flip-flop 4J-11 in a high state, and the next clock pulse places flip-flop 4J-8 in its high state. NOR gate 3K-12 senses the one clock width interval when 4J-11 is high and 4J-8 is low, resulting in a positive pulse, one clock period in duration. This pulse combines with the clock in OR gate 3K-10 to effectively delete one clock pulse.

On sheet 9 the suppress leading zero logic is shown. The function of the suppress leading zeros logic is to prevent strings of consecutive zeros of lengths greater than 14. Since strings of greater than 14 zeros do not occur with PR sequences of lengths M=9, 11, and 15, the suppress leading zero logic only functions for PR sequences of lengths M=20 and M=23. For each zero which exceeds 14, the suppress

leading zero logic, when activated by the SUPLDO command, outputs a high level signal 3K-4, which forces the former leading zeros to ones. For example, a string of 17 consecutive zeros results in a signal of 3-bits duration, and forces the first three zeros to ones.

The suppress leading zero logic is implemented using a divide-by-16 binary up-counter module 1J, and 3 gates module 3K. In order to describe operation, consider an example which includes a string of 17 consecutive signals. The second stage of the transmit pattern generator shift register is inverted by module 2K-4 and applied to the S1 and S2 mode control inputs of counter module 1J. Zeros in the data permit the counter to increment, while ones synchronously load the counter to its zero state. When the first zero occurs, the counter increments to state one, the second zero increments the counter to state two, and so on, until the fifteenth zero increments the counter to its terminal count of state fifteen. The terminal count output is inverted by module 3K-8 and applied as a STOP signal to the count enable input. Because the TC (terminal count) pin becomes low when a load command is set up at S1 and S2 of the chip, terminal count is wire-ORed with the $\overline{Q}$ outputs of the counter, which prevents false terminal counts during loading and the introduction of false ones into the data stream. At this point, the counter stays at its terminal count for the remaining consecutive zeros, and a high signal, three bits in duration, results at the output of NOR gate 3K-4. The high signal is combined with the output of stage 17 of the transmitter pattern generator shift register output in OR gate 3K-2. This signal is delayed by 15 bits from the stage 2 signal. The high signal generated, always commences one bit after the 15th zero of the stage 2 signal and continues until one bit after the first one.

Logic required for data inversion is also located on sheet 9. Inversion is controlled by the $\overline{\text{TRUPATT}}$ setup register bit, which is combined with the transmitted data using EXCLUSIVE-OR gate 2K-9. A high level input signal thus inverts the data upon operator selection of TXPOL (Transmitter Data Polarity) command.

Input signals FORCE 1 and FORCE 0 are applied to the set and clear inputs of D-type flip-flop 2J-8, respectively, as shown on sheet 9. Either input signal is capable of overriding the normal transmitted data.

4.4.2.8 Control Bus Logic. The I/O control bus logic, located on the transmitter board, is shown on sheet 10. A negative level on the $\overline{\text{CNTRDY}}$ signal indicates the presence of a valid input control signal on the 8-bit control bus CBØ through CB7. The negative transition of the $\overline{\text{CNTRDY}}$ signal passes through 5E-16, and is inverted by 3C-3, triggering flip-flop 3E-5 to a low state. The low level signal is applied to 8-bit shift register 4D, which is clocked by the 5.6 MHz

clock. The QB register output sets flip-flop 3E-5 to a high state, creating a negative pulse, two-bits-wide (357 nanoseconds), which is shifted through the register. The positive transition at QA transfers the control bus signal into the octal, D-type register 5C. Outputs of this register are decoded to form all of the necessary write/read commands and control signals. The first control bit, CBØ, is the write/read control signal. Control bits CB3-CB6 represent, in binary form, one of sixteen possible control words (only 9 are presently used). The second and third bits, CB1 and CB2, can be used to further divide each control word into four separate bytes A, B, C, and D.

When W/R is high, one of the nine write signals, $\overline{WØ}$ through $\overline{W8}$, goes low, while QD of 4D goes low. Signals $\overline{WØ}$ - $\overline{W7}$ are decoded by the output of 5B; $\overline{W3}$ is decoded using module 3C. Using module 4C and the byte select signals, $\overline{W4}$ is further decoded to form $\overline{W4A}$, $\overline{W4B}$, and $\overline{W4C}$. When W/R is low, decoder module 5A is active. The five read signals, $\overline{R1}$ through $\overline{R5}$, are decoded to appear as negative levels, when selected. Signals $\overline{R1}$, $\overline{R2}$, and $\overline{R3}$ are further decoded using modules 4A and 4B, which have byte select signals as inputs. When QB at 4D-4 returns to a high level, the W/R signal is transferred to flip-flop 3E-11, which controls the direction of data transfers, as specified by the W/R control line. When QH at 4D-13 goes low, 3E is placed in a set state regardless of the state of W/R. When W/R is low, the $\overline{Q}$ output of 3E is combined with positive pulse $\overline{QE}$ at gate 3D-6, which is buffered by 5E-12 to form the $\overline{DATARDY}$ signal. This signal disables the data bus drivers on the processor board to allow data to read from the transmitter board.

4.4.2.9 Data Bus Logic. The data bus logic is shown on sheet 11. Designed as a bidirectional octal bus, the data bus conveys data in both directions between the transmitter and receiver boards and the processor board. The direction of the data is controlled by the $\overline{OE}$ and OE signals applied to module 2C, which is used as a tri-state, octal, line driver. When OE is high, module 2C is enabled and the contents of the TTL output bus are placed on the data bus. When OE is low, module 2C is placed in a tri-state condition. Incoming data bus signals pass through the octal line receiver module 2B to the D-type octal input register 2D. The clock input to 2D is the QB signal from sheet 10. When QB goes from a low to a high state, data bus signals are transferred into 2D.

The outputs of register module 2D are the eight TTL input bus signals TTLIBØ through TTLIB7. These signals are routed through connector JB (sheet 16) to the receiver board (sheet 18 of 500-0731) to six TTL octal registers. The TTL input bus signals are also converted to ECL level signals via modules 3FF, 4FF, 2G, and 3G to form the eight ECL input bus signals. These signals are routed to ECL octal registers, shown on logic sheets 7, 12, and 14, and also through connector JB to the receiver board, where the signals appear as inputs to additional registers.

On sheet 11, tri-state octal driver, module 2-C is used to place the eight TTL output bus signals TTLOBØ through TTLOB7 on the data bus. In addition to module 2C, outputs from twelve other octal tri-state storage register modules are connected to the TTL output bus. Six of the modules, 7A, 7B, and 7C on sheet 3, and 10A, 10B, and 10C on sheet 4, are located on the transmitter board. The outputs from the remaining six modules, located on the receiver board, are routed to the transmitter board.

4.4.3 RECEIVER BOARD (GPO31-1; Logic Diagram 500-0731, sheets 1-18)

The primary function of the receiver board is to accept and measure the quality of the incoming clock and data. The receiver logic, in order to monitor the parameters, must be capable of establishing its own reference generator relative to the incoming data, and maintaining synchronization in the presence of data link errors. Specific parameters which are monitored by the receiver are bits, blocks, errors, error rate, bad blocks, and seconds; the following paragraphs describe the logic for monitoring these parameters.

4.4.3.1 Bit Prescaler and Run Control Logic. Sheet 1 of the logic diagram shows the bit prescaler. The bit prescaler includes a counter module 9K, which divides the receiver clock by either 10 or 16. The actual divisor is determined by the polarity of input signal P16/10 which is applied to parallel inputs P1 and P2 of the counter. When P16/10 is in its high state the counter is synchronously loaded to state 15; when P16/10 is low, the counter is loaded to state 9. The BITTC signal is connected to QØ of module 9K, which is necessary since BITTC goes to a low state during load, as well as when terminal count is reached. This signal and the NEW RUN signal are applied to module 9J. The output of this module is applied to control input S2 of 9K. When this signal is high, the module counts down; when the signal is low, it synchronously loads the counter.

Module 9J-11 serves as a 2-input multiplexer for the receiver clock RTO and the Q3 output of the prescaler counter. This multiplexer is controlled by the SLHIRT (Select High Rate) signal. When the clock rate exceeds or equals 10 megabits, the prescaled clock is selected. The output of this multiplexer is referred to as the bit clock. For high rates the bit clock is the receiver clock divided by either 10 or 16; for low rates it is the receiver clock RTO directly. This output, referred to as BITCKE, is converted to TTL level at 8FF-4 to form BITCKT. Module 9H-11 is also a 2-input multiplexer. The two signal inputs to this multiplexer are BITCKE and HZlECL. The multiplexer is controlled by the BITMDE control signal. Module 6FF-12 converts the multiplexer output to the TTL level signal BTSCLK. Note that when the NEW RUN signal is in its low state, the BITCKE, BITCKT and BTSCLK signals are inhibited (held in their low state).

Sheet 1 also includes the run control logic. This logic forms the NEW RUN signal at flip-flop 7L-4. When NEW RUN is low, BITCKE, BITCKT, and BTSCLK are inhibited via gates 9J-11 and 9H-11. The NEW RUN signal is applied as a count enable (inverted) input to the bad block threshold logic error counter 6H (sheet 5) and to the error prescaler counter 7H (sheet 3), forcing these counters to the hold mode between runs. Between runs the RUN control signal to NOR gate 7J-11 is held high, which keeps NEW RUN low since the output of 7J-11 is the input to flip-flop 7L-4. The second input to 7J-11 is the ALWRSE signal. This signal goes high when a loss of sync occurs; a loss of sync at any time during or between runs will cause NEW RUN to go low, inhibiting operation. The NEW RUN signal is synchronized to either RTØ or HZ1ECL depending on control signal BITMDE since the clock input to 7L-2 is the output of multiplexer module 9J-8. A high level from 6G-5, caused by the EOTT signal, clears 7L-4 forcing NEW RUN to its low state.

4.4.3.2 Bits/Block and Seconds/Test Counter and End of Time Test Logic. The bits per block and seconds per test counter logic is shown on sheet 2 of the logic diagram. The counter is a five-stage, programmable, synchronous, binary counter which is used to count bits/block or seconds/test. The BITMDT control signal regulates the counter which may be programmed to count by any number from 1 to $2^{20}-1$, using the 20 control inputs BBØ through BB19 in ones complement form.

The end of time test logic is also shown on sheet 2. The purpose of this logic is to generate the EOTT signal. This logic is only operable when the BITMDE control signal is low, which signifies the continuous mode and seconds mode. Between tests the MRT signal sets flip-flop 9X (sheet 1) to its high state through 10C-13, therefore, EOTT is low. Assuming BITMDT and MRT are both low, a positive transition on EOTT will force 9X-8 (sheet 1) and 6G-4 (sheet 1) high, causing NEW RUN to go low. The EOTT signal is a negative pulse with a duration of one-half second which occurs when the seconds per test counter reaches its terminal count.

4.4.3.3 Bits/Block and Seconds/Test Modes. When in the bits per block mode, the function of the counter is to continuously count down its input clock to form the block rate. Between tests, the BTSCLK is held in its low state, and D-type flip-flop module 13X-A is cleared by the MRT signal. This forces the counter load (LD) inputs to a low state. The counter is thus loaded to its initial state by the first clock, which occurs at the beginning of each new run or test. The counter is incremented by each successive clock until terminal count is reached; terminal count is sensed by module 10X. When terminal count occurs, the load signal at 11D-13 goes low and the next clock synchronously loads the counter to its initial state. This process is continuous until the test is ended. The individual terminal count output signals

from modules 13A through 13E are sensed by NAND gate 10X to insure operation for all divisors to rates in excess of 10 megabits. When in the bits/block mode, the inverted terminal count is gated through modules 9B and 9C to become both the BKSCLK and the GBGATE signals. The BKSINT monitor signal is derived by flip-flop 13X whose output is a 50% duty cycle at one-half the block rate.

When in the seconds/test mode operation of the counter is essentially the same as described for the bits/block mode. The essential differences are that the clock is at a 1 Hz rate and when terminal count is reached, for the first time, the test is stopped. This is accomplished by combing the sensed terminal count with the clock to form signal EOTT (End of Timed Test). The positive edge of this signal is used to end NEW RUN and thus stop the BTSCLK. When in the seconds/test mode, the HZ1 (TTL) signal is gated through modules 9C, 9B, and 8X to become the BKSCLK signal. This signal is applied to toggle flip-flop 13X to form the INT signal at a rate of 1/2 Hz. An inverted version of the HZ1 (TTL) signal is gated through modules 9B and 9C to form the GBGATE.

4.4.3.4 Error Prescaler and Reset Logic. The error prescaler logic is shown on sheet 3 of the logic diagram. The logic consists primarily of three, 4-stage counter shift register modules, 7H, 7G, and 8G. Module 7H is connected as a divide-by-16, synchronous, binary counter; module 7G is a storage register; and module 8G is used as a counter/synchronizer. When in the continuous mode, module 7H is simply used to count errors; the counter increments by one when an error occurs. The contents of counter 7H are transferred synchronously to holding register 7G whenever the BITTC signal is low. This signal is the terminal count output of the bit prescaler. When in the high rate mode, BITTC goes to its low state either every 16 or 10 clocks, depending on control signal P16/10, transferring the contents of 7H to 7G. When in the low rate mode, the BITTC signal remains low and the contents of 7H are continuously transferred to 7G. The function of modules 8G, 7J-12/13, 7J-8, 5K-11 and 6L-4 is to synchronize the error prescaler to the bit prescaler. The terminal count output of module 7H is applied to pin 14 of module 7J. The noninverted output at pin 13 of 7J is the count enable input of module 8G. When each 16th error occurs, counter 8G increments by one. The inverted output of 7J-11 is applied to the PØ input of 8G to handle the case where the 16th error occurs when the BITTC signal is in its low state. Since BITTC is an input to control signals S1 and S2, of module 8G, this counter is synchronously loaded, when BITTC is in its low state, to either zero or one (if 16th error occurs). Therefore, counter module 8G may or may not be incremented to state one during each bit prescaler interval depending on whether or not the 16th error should occur during that particular interval. Assuming the 16th error did occur during a particular bit prescaler interval, the QØ of module 8G will be low. This signal is combined with BITTC in NOR gate 7J-8. The clock pulse which follows will cause D-type flip-flip module 5K-11 to go to its high level state for one period. This high level signal is used to set flip-flop 6L-4, setting the ERR16 signal to its

high state. The ERR16 signal, which is now synchronous with the bit prescaler signal, is used as a clock for the error counter. Module 7FF is an ECL to TTL converter which converts the output of holding register 7G to TTL level. This TTL level signal, which represents the error "residue," can have any value from 0 to 15, and is used as an input to the error counter register.

Sheet 3 also shows the reset logic. The ECLRST input signal is retimed using the receive timing clock RT4 at flip-flop 4G-4 to form MRE. The signal MRE is the ECL level master reset signal used to clear the error prescaler and the bad block threshold logic on sheet 5. Module 4FF-5 converts this signal to TTL level. The output of 4FF-5 is buffered using module 5C to form $\overline{MRT}$ and MRT. These signals are used to initialize counters between runs.

4.4.3.5 Error Counter. The error counter logic is shown on sheet 4 of the logic diagram. The counter is a six-stage, synchronous binary counter capable of counting up to $2^{24}-1$. Since the error count is prescaled by 16, up to $2^{28}-1$ errors may be counted. When in the continuous mode, as controlled by the CNTEST input signal, the counter contents (28 signals) are transferred to the four D-type, octal, tri-state latches, modules 11C, 11B, 11A, and 11X by the latch error signal at 11D-4. This transfer occurs after each negative transition of BITCKT, as long as signal $\overline{L3}$ remains in its high state. The ERR16 clock is synchronous with the BITCKT signal. When $\overline{L3}$ goes to its low level state, any subsequent latching is inhibited. As long as $\overline{L3}$ remains in its low state, the ERRDST (Error Read Status) flag is reset to its low level state. The first latch signal which occurs after $\overline{L3}$ goes to its high level state causes the ERRDST signal to its high level state. Signals from the four error counter latches may be transferred to the TTL output bus by the four output enable signals $\overline{R3A}$, $\overline{R3B}$, $\overline{R3C}$ and $\overline{R3D}$.

4.4.3.6 Error Rate Interval Transfer Logic. Sheet 4 also includes the error rate interval transfer logic. This logic is used to generate $\overline{SYNLD}$ signals. Figure 4-8 illustrates the timing waveforms for each of the different signals in both the high and low rate modes. When in the high rate mode, combining the ERRINT signal on sheet 6 with the BITTC signal in OR gate 7J-13 yields a $\overline{SYNLD}$ signal which has the duration of one received clock period (RT). The output of the $\overline{SYNLD}$ signal is applied to the error prescaler at the mode control inputs S1 and S2 of the counter module 7H on sheet 3, which places the counters in the synchronous load mode when $\overline{SYNLD}$ is in its low level state. At the beginning of each new error rate interval, this bit effectively resets counter 7H, also on sheet 3. The ERROR signal is applied to the PØ parallel input of the 7H counter, causing it to be reset to state zero if there is no error. However, if an error should occur in the first bit of the interval, the counter will reset to state one. The output of the $\overline{SYNLD}$ signal on sheet 4 is also applied to the

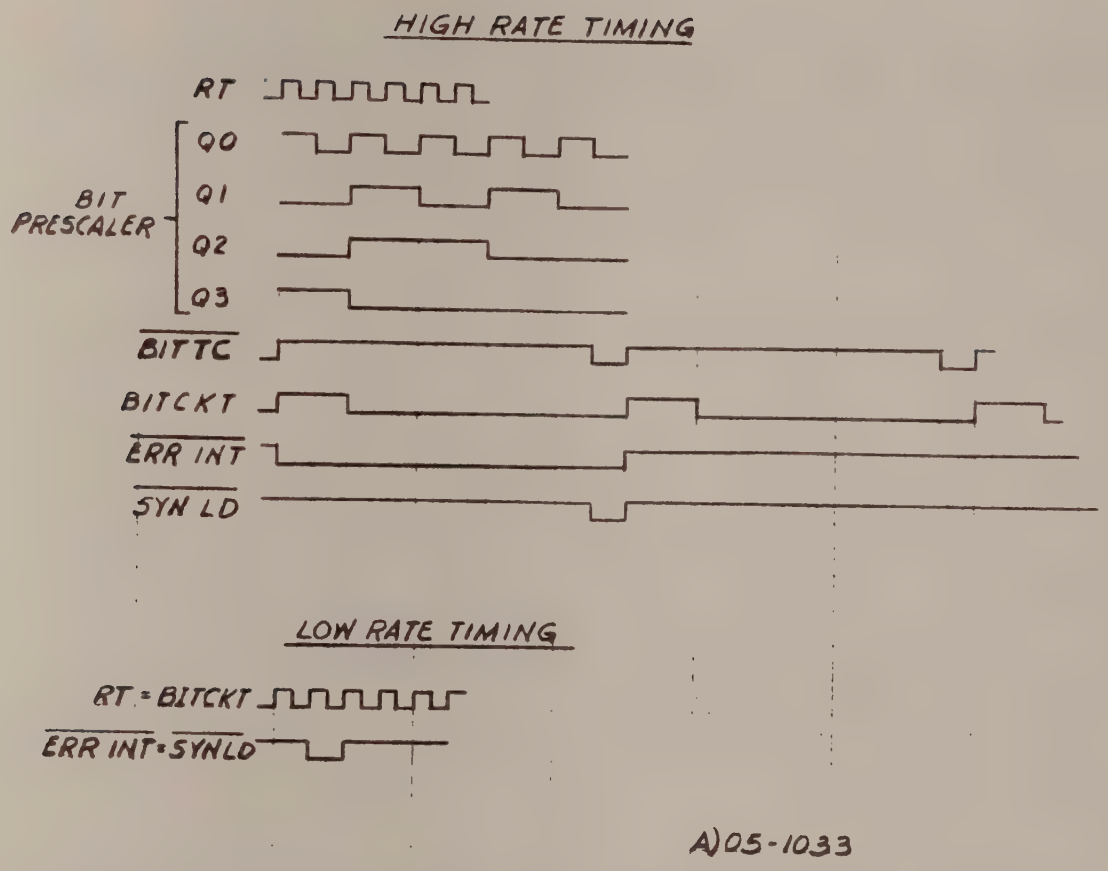


Figure 4-8. Error Interval Timing Waveforms

clock input of D-type flip-flop module 8J-A. The Q output of this flip-flop is applied to the D input of flip-flop 8J-B, which is clocked by BITCKE. When in the low rate mode, RT0 and BITCKT are at the same rate, resulting in the SYNLD signal shown in Figure 4-8.

4.4.3.7 Bad Block or Seconds Threshold Logic. The bad block or bad seconds threshold logic is shown on sheet 5. The function of this logic is to determine on either a block-by-block or a second-by-second basis (as controlled by the BITMDE control input) whether or not the number of errors which occur in a given block/second equal or exceed a number defined by a programmable binary input. Each block/second is labeled as either good or bad. The bad block or seconds threshold logic outputs a pulse (BBSCLK) each time a block/second is bad.

During each block or second interval, the number of errors is counted using module 6H. At the beginning of each interval a one-bit-wide pulse is applied to the control inputs S1 and S2 of module 6H, which synchronously loads this counter to either state zero or state one depending on whether or not an error occurs in the first bit of the interval. For each subsequent error, the counter will increment by one until it either reaches its terminal count, or until the beginning of the next interval. Should terminal count be reached, the counter is held in this state by forcing the count enable input CP to a high level state. The same one-bit-wide pulse which synchronously loads counter module 6H, also is applied to control inputs SØ, S1 and S2 of module 6G. This module serves as a holding register for the contents of module 6H. At the beginning of each interval, the contents of 6H are synchronously loaded into module 6G. The outputs of 6G are converted to TTL level via module 6FF. The TTL level binary signal, which represents the number of errors which occurred in the interval, is compared to the programmed input represented by inputs BBIØ, BBI1, BBI2, and BBI3, using 4-bit comparator module 9E. When the actual error count is greater than or equal to the programmed input, the comparator output goes to its low state signifying a bad interval (block or second). This results in a pulse, BBSCLK, at the output of gate 10C-10. Each pulse toggles D-type flip-flop 9X resulting in a transition at the output of BBMON (Bad Block Monitor) module 5B. Figure 4-9 illustrates the timing waveforms for the bad block/seconds threshold logic. When in the seconds mode, the GB GATE becomes the HZ1 signal inverted, which is also noted in Figure 4-9. A decision of whether or not each second is good or bad is made using the first clock, RT, which occurs after the end of each second.

4.4.3.8 Error Interval and Suppress Leading Zero Logic. The error rate logic bit counter is shown on sheet 6. The function of this logic is to provide the ERRINT signal required for error rate calculations. The logic consists of an 8-decade synchronous counter, an 8 input multiplexer, and a 2-input NAND gate. The eight counter stages, modules 6E, 6D, 6C, 6B, 6A, 6X, 7E and 7D, are synchronous 4-bit decade counters. The terminal counts of the last seven stages

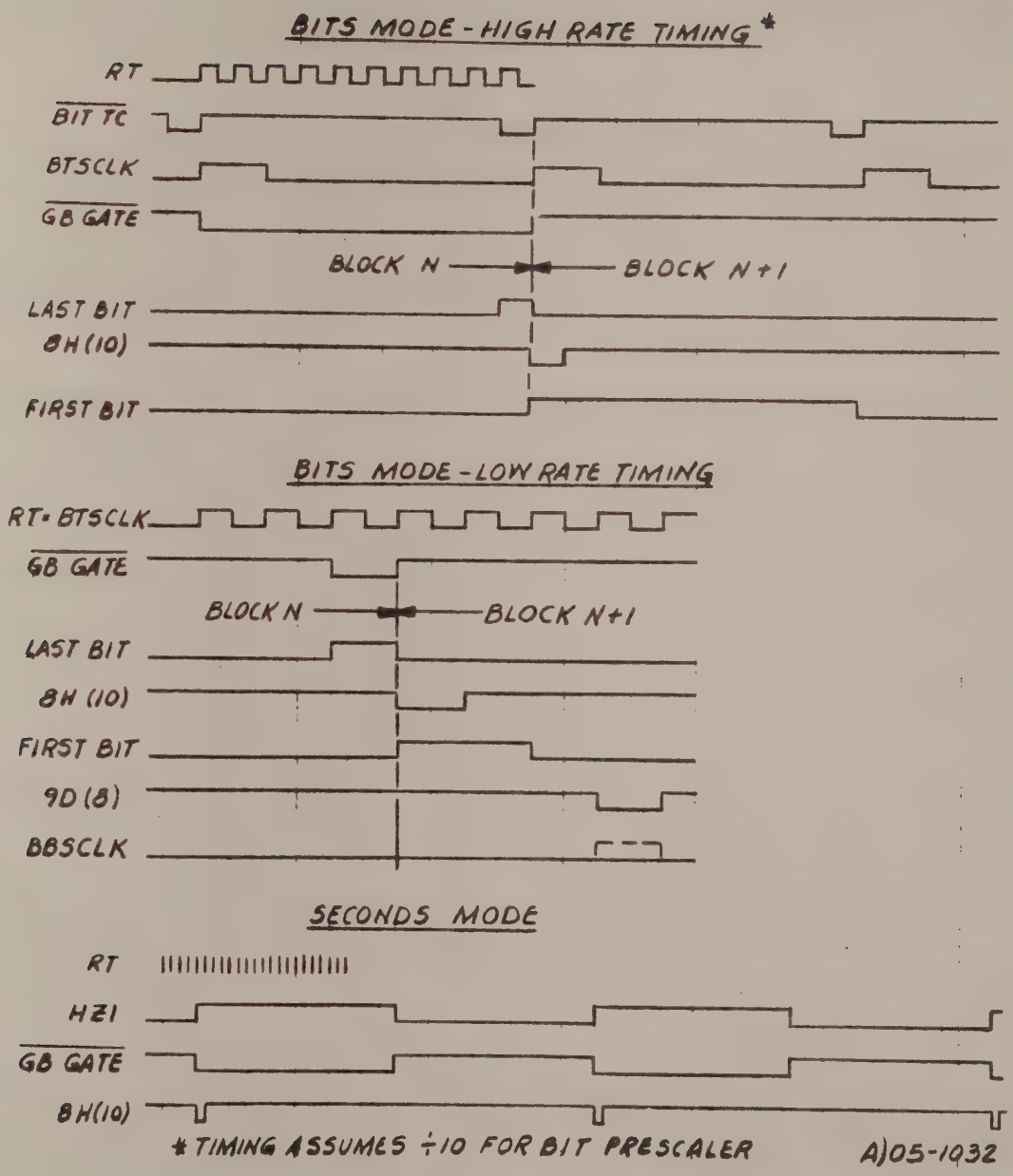


Figure 4-9. Bad Block/Second Threshold Logic Timing Waveforms

are inputs to the multiplexer module 7X. Each of these outputs has a duration of ten BITCKT periods. The terminal count output of module 6E has a duration of one BITCKT period. When this output is combined with the multiplexer output using NAND gate 11E, the gate output signal ERRINT always has a duration of one bit clock period. The ERRINT signal can only occur when the CNTST signal is in its low level state. Table 4-13 lists the bit interval as a function of the multiplexer control signals.

Table 4-13

Comparison of Bit Interval and Multiplexer Control Signals

Mode Input	Control Inputs			Bit Interval	
CNTEST	10E4	10E2	10E1	With Bit Prescaler*	Without Bit Prescaler
0	0	0	0	10^2	10^1
0	0	0	1	10^3	10^2
0	0	1	0	10^4	10^3
0	0	1	1	10^5	10^4
0	1	0	0	10^6	10^5
0	1	0	1	10^7	10^6
0	1	1	0	10^8	10^7
0	1	1	1	10^9	10^8
1	X	X	X	None	None

* Assumes prescaler divides by 10 (not 16).

The suppress leading zero logic is also shown on sheet 6. This logic performs the dual role of the functions described in paragraph 4.4.2.7 of the transmitter board logic, Section 4.4.2. The leading zeros, suppressed at the transmitter board, must be re-inserted at the receiver board, prior to their appearance at the receiver open loop register. When the ENSUPO control signal is low, the suppress leading zero logic is activated. Thus, when $\overline{TC}$ of module 1K goes low, the SUPRSO signal goes high, inverting the data signal via EXCLUSIVE-OR gate 4K-3 shown on logic sheet 11. Inverting the data, rather than forcing ones has the effect of retaining any errors which may have occurred in the received data bits. On the transmitter board, stage seventeen of the pattern generator shift register was combined with the signal which suppressed leading zeros, and the inverted signal from stage two was used as the control input to the counter. This same timing relationship must be retained by the receiver logic. Since the input to EXCLUSIVE-OR gate 4K-3 is delayed one bit relative to RDATA, the signal at the input of counter module 1K must be advanced relative to RDATA by fourteen bits. The suppress leading zero logic is only active for the normal PN sequences, N=20 and N=23. For N=20,

the proper required input for the counter input can be generated by the EXCLUSIVE-NOR combination of stages two and seven of the closed loop register. Also, SL1 is at its high level state, causing the signal at pins 9, 11, and 15 of module 2J high. The control output of the counter becomes the inverted output of 2J-1. Similarly, for N=23, stages one and four are combined. SL0 goes to its high state and the control signal becomes the inverted output of 2J-1.

4.4.3.9 Receive Timing and Data Selection Logic. Sheet 7 illustrates the logic for selection of the receiver timing and data. The receiver board provides for selection of any one of three timing and data sources. These three sources are the receive data and timing (normal operation), transmit data and timing (loopback testing), and a special mode for operation with 50 kb data.

a. Receive Data and Timing (Normal Operation). For normal operation, the Loop Test (LOOP TEST) and Select 50 kb (SEL50K) control signals are in their low states. The receive data and timing signals enter the receiver board via coaxial connectors JC and JD. These balanced signals are at an impedance of 50 ohms (25 ohms per side). Two parallel multi-wire signal paths are needed for each of the four signals. Differential line receivers 9L-13 and 9L-11 eliminate any common mode noise and convert the signals to balanced form. The timing signal then passes through EXCLUSIVE-NOR gate 9M-10 and multiplexer gate 8M-8 to D-type flip-flop 8J-4. The data signal passes through gates 9M-13 and 9M-3 before appearing at flip-flop 8J-4. These modules are included in order to balance out the delays encountered by the timing signal. For normal timing, the positive clock transitions coincide, or slightly precede, data transitions. The INVRT signal is normally low, causing the clock to be inverted at module 9M-10 and the data to be center sampled at 8J-4. The clock is then routed through module 8M-4 to gate 8L, whose outputs are the six receive timing clocks. The retimed data at the output of 8J-4 is routed through gate 9M-9 to form RDATA. However, if the INVRT control signal is in its high level state, the data is inverted.

b. Transmit Data and Timing (Loopback Operation). Data and timing signals from the transmitter board are routed, in balanced form, to the receiver board. Differential line receiver modules 5G-3 and 9L-3 convert these signals to unbalanced form. When the LOOP TEST control signal is at its high level state, these signals are routed through modules 8M-4 and 8M-11 to form RDATA and RTØ through RT6.

c. 50 kb Operation. When in the 50 kb mode, received timing does not exist. The received 50 kb data, at the output of module 9M-3, is converted to TTL level by module 9FF-4. The TTL level signal is routed to the transmitter board via pin 39 of connector JA, where a clock is developed.

4.4.3.10 Open Loop Register Logic and Reference Generator Shift Register Logic. Sheets 8, 9, and 10 show the receiver open loop register and reference generator shift register respectively. Operations of these registers is similar to operation of the transmitter pattern generator described in paragraph 4.4.2.7. The 24-bit open loop register is implemented using three, 8-bit shift register modules, 4N, 4M, and 4L. The data input, RDAT1D, is a delayed version of the input data discussed in paragraph 4.4.3.11.

The reference generator shift register is also implemented using three, 8-bit shift register modules, 4N, 4M, and 4L. The serial input to this closed loop register is the output of EXCLUSIVE-OR gate 2K-13, REFDAT on sheet 10. This signal is formed by combining the outputs of multiplexer modules 1L and 1M, as controlled by the eight control signal inputs SLØ through SL3 and STØ through ST3. The reference generator also includes provision for a parallel load. When the $\overline{\text{PRIME}}$ signal, connected to control input SØ of the three 8-bit shift registers 3N, 3M, and 3L on sheet 9, is in its low level state, the registers are synchronously loaded. The 24 parallel inputs are the corresponding outputs of the open loop register. The reference generator signal is thus delayed by one clock period relative to the open loop register signal. The open loop register outputs also go to length and tap multiplexers, modules 5N and 5M. Their outputs are combined using EXCLUSIVE-OR gate 2K-11 to form the predicted value PREDAT on sheet 10.

4.4.3.11 Error Detection Logic and Pattern Sync Logic. The error detection logic is included on sheet 11. The function of this logic is to compare the incoming data with the REFDAT and PREDAT signals to form the ERROR and $\overline{\text{PE}}$ signals. The closed loop REFDAT is retimed using the Q1 stage of module 5L. RDATA must be delayed by three clock periods in order to coincide correctly in time with the retimed REFDAT signal. This is accomplished using D-type flip-flops to form RDAT3D. Retimed REFDAT and RDAT3D are compared using EXCLUSIVE-OR gate 4K-13. The output at 4K-13 is retimed using 5L-5 to form the ERROR signal. The predicted value from the open loop register is retimed via 5L-Q2, and the retimed output is then compared with RDAT1D using EXCLUSIVE-OR gate 4K-11. The output of 4K-11 is retimed via 5L-2 to form the $\overline{\text{PE}}$ signal.

The receiver pattern sync logic is also shown on sheet 11. The 24 outputs of the closed loop receiver reference generator are compared to the 24-bit reference word from the reference word register located on the transmitter board. These signals are sent between logic boards using pins 25-48 of connector JB. Operation of the receiver pattern sync logic is identical to the transmitter pattern sync logic described in paragraph 4.4.2.6.

4.4.3.12 Sync Control Logic. The sync control logic consists of the sync error prescaler and counter, the sync bit prescaler counter,

the test control logic, the predictor error counter, a flat line detector, the sync tries counter, and resync control logic. The sync control logic is shown on sheets 12, 13 and 14 of the logic diagram.

The test interval counter consists of ECL sync bit prescaler counter 5H and binary counter 1E on sheet 12. For PN patterns, 1X-9 goes high after 128 bits, unless 32 or more predictor errors occurred (PEGT32 is high). If 32 or more predictor errors occurred, 1X-9 is held low via 2C, and the sync test is extended from the SHORT test (128 bits) to the MEDIUM test. If 1X-9is allowed to go high at 128 bit times, an in-sync or out-of-sync decision is made based on the state of flip-flop 1B-5 by gate 2D-8. If 48 or more bit errors occurred during the 128 bit test interval, 2D-8 sets flip-flop 2X-5, which results in the Allow Resync (ALWRSE) state. If less than 48 errors occurred, 2D-8 remains high and the sync test is halted through 2B-3 when 1X-9 goes high. Whenever an ALWRSE state exists, the low output from 2X-6 holds flip-flop 5K in its set state, via 5FF-15 and 5G-9, preventing any further sync tests until sync is acquired. The status of the sync flip-flop 2X-5 is shown by the RSYFLG output of flip-flop 2X-9 and the Resync Monitor Signal (RSNMON) at 5C-1. The resync status signal is supplied to the status register shown on sheet 17 as ALWRSE. If no decision is made at 128 bit times, 1X-5 goes low at 512 bit times, unless 192 or more bit errors occurred. If 192 bit errors occur, 1B-9 goes high causing 2C-1 to go low, and holding 1X-5 high. If 1X-5 is allowed to go low (<192 bit errors in 512 bit times), the sync test is terminated through 2A-8; otherwise, the sync test is allowed to extend from the MEDIUM to the LONG test. At 1536 bit times, 1A-9 is high and an in-sync or out-of-sync decision is made. If less than 720 bits occurred, 1A-6 goes high, and the sync test is terminated through 2B-6. If 720 or more bit errors occurred, 2X-5 is set by 2D-8. The output from 2X-5 then clocks 2X-8 and passes through 1FF-1 and 1G-3 to provide the ALWRSE signal. At any time before 1536 bit times, the sync test can be terminated by a low $\overline{\text{STOP 2}}$ signal indicating that 720 predictor errors occurred. Any termination of the sync test sets 5K-8, clearing the error and test interval counters. A new test can be initiated following the next bit error. In the word mode, 1B-9 and 1X-5 are held preset, disabling the MEDIUM (512 bit) sync test. Through 2D-6 and 2B-8, the SHORT test is extended from 128 to 1024 bits.

The test control logic consists primarily of gate 2A and flip-flop 5K on sheet 12. When the flip-flop is in its high state (test off), all counters associated with the sync test are held in a clear or initialized state. When a bit error occurs, the high ERROR signal causes 5K-8 to go low, enabling the test interval and error counters. The bit error counter consists of an ECL binary counter 5J and TTL binary counter 1E. If 48 or more errors occur, 1B-5 is set; if 192 or more errors occur, 1B-9 is set; and if 720 or more errors occur, 1A-5 is set. These outputs establish the closed loop error thresholds.

The predictor error counter consists of ECL binary counter 4J, and TTL binary counters 3E on sheet 13 of the logic diagram. If 32 or more predictor errors occur 3D-6, goes high. If 720 predictor errors

occur during the sync test, 3D-9 goes low. The $\overline{\text{STOP 2}}$ signal indicates that the line data is corrupt and sets 5K-8 via gate 2A-4 on sheet 12, stopping the sync test.

Counter 4H and associated flip-flops and gates on sheet 13 form the flat line detector which prevents a sync test from starting, or terminates a sync test in progress if a flat data input is detected. EXCLUSIVE-OR gate 4K-9 compares the received data and the data delayed by one bit, at 5K-4 to detect data transition. For each non-comparison, flip-flops 4G-11 and 4G-8 are preset and counter 4H is cleared; for each comparison 4H increments. After 8 consecutive comparisons, Q3 goes high triggering 4G-11 to a high state. After an additional 16 consecutive comparisons, 4G-8 goes high to provide the low $\overline{\text{STOP 1}}$ signal at the output of 2B-11. The output of the flat line detector at 2B-11 is inhibited when control signal $\overline{\text{PAT10}}$ is in a low state.

The resync logic consists of binary counter modules 3H and 3G, along with gates and flip-flops shown on sheet 14. The counter is a binary down counter whose count is programmable via the eight binary input control signals RSLØ through RSL7. The predictor error signal $\overline{\text{PE}}$ is applied to counter control input S2. When an error occurs, the counter is synchronously loaded with signals RSLØ-RSL7. For each errorless bit, the counter decrements. Terminal count is reached only when the number of consecutive errorless bits equals the value of the input control signal. The counter remains at terminal count until the next error occurs. When an out-of-sync condition exists, the ALWRSE signal is high. If the counter decrements to its terminal count, flip-flop 2H-11 goes high. This high level is clocked through a 3-stage shift register consisting of 2G. Since 2G-4 is fed back to clear 2H, a 3-bit-wide high level signal occurs. The outputs at 2H-10 and 2G-10 are sensed by OR gate 1J-9 to form a 2-bit period low level signal $\overline{\text{PRIME}}$ at 1J-9. This low $\overline{\text{PRIME}}$ pulse is applied to the reference generator to synchronize it, by transferring error-free data stored in the predictor register. The $\overline{\text{SYNPLS}}$ signal also goes low for 3 bit periods, which increments the sync tries counter and clocks flip-flop 2X-5 on sheet 12, forcing ALWRSE back to its low state.

The sync tries counter consists of counter modules 3B and 3C on sheet 14. While in the run state, this counter increments by one, each time a loss of sync occurs. When the signal at 2C-4 goes low, the counter is inhibited. A low at 2C-4 occurs when either the counter reaches its terminal count or when a halt occurs. During halt, RUN goes low, passes through 8X-11 and 2C-4, and stops the counter. The eight sync tries counter outputs RSTRYØ-RSTRY7 go to the resync tries register on sheet 17.

4.4.3.13 Receiver Signal Monitors and Receiver Status Monitors. The receiver signal monitors are listed in Table 4-14. Each of these signals is buffered using a 50 ohm TTL line driver module. At location 5X, these signals are each connected to separate pins.

Table 4-14

Receiver Signal Monitors

Signal Name	Functional Name	Buffer Driver	Output Location	Sheet Number
BKSINT	Block or Seconds Interval Monitor	5B	5X-7	2
BBMON	Bad Blocks Monitor	5B	5X-2	5
RDMON	Receive Data Monitor	10A	5X-8	7
RTMON	Receive Timing Monitor	10A	5X-9	7
ALARM	Alarm	10A	5X-6	7
ERRMON	Error Monitor	5B	5X-3	11
RPATSY	Receive Pattern Sync Monitor	5B	5X-4	11
RSNMON	Resync Monitor	5C	5X-5	12

The receiver status monitor signals are listed in Table 4-15. All eight of the status monitor signals are connected as inputs to tri-state, octal, register, 5E, located on sheet 17.

Two TTL versions of received data (RDMON) and timing (RTMON) are available. Activity monitors test for a transition of data and clock each second. The signals, RDOK and RTOK indicate respectively, the status of RD and RT. If either RD or RT are not present, the ALARM signal will appear. The receiver sync status is indicated by RSNMON (Receiver Sync Monitor).

Two signals are generated to indicate data is available to the processor board: BCRDST (Block Counter Read Status) and BBRDST (Bad Block Read Status). Each signal is set when test result data is available, and remains set until the processor board inhibits further updating by "latching" the data.

Table 4-15

Receiver Status Monitors

Signal Name	Functional Name	Board Location	Sheet Number
RDOK	Receive Data OK	GPO31-1	7
RTOK	Receive Timing OK	GPO31-1	7
ALWRSE,	Allow Resync ECL,	GPO31-1	12
ALWRST	Allow Resync TTL	GPO31-1	12
RSYFLG	Resync Flag	GPO31-1	12
BBRDST	Bad Block Read Status	GPO29-1	7
BCRDST	Bad Clock Read Status	GPO31-1	4
ERRDST	Error Read Status	GPO31-1	3

4.4.4 INTERFACE BOARD (INF014-1; Schematic 460-1658-501, sheets 2 and 3)

The clock (TT) and data (SD) signals are connected through coaxial cables to the GPO29-1 transmitter board, designated A5. A differential signal is received by the line receivers U9 at pins 20 and 21 for clock, and pins 16 and 17 for data. The outputs of these line receivers are connected to U2, a line driver which delivers a differential signal to J3 through J6. The points J3-J6 are connected to the rear panel via coaxial cables. These lines should be terminated by 100 ohms, line to line from TTA and TTB, and from SDA and SDB.

The line driver U2 also contains additional outputs. The OR outputs U2-8 and U2-15 are connected to U2-21 and U2-20. The OR/NOR outputs U2-23 and U2-24 are connected to the bases of transistors Q4 and Q5. Circuit configuration Q5, Q4, Q3, Q2, Q1 and U13-7 is a nonsaturating TTL line driver. Current is steered through Q4 or Q5 when the associated base is a high ECL level of approximately -0.9V. When Q5 is turned on, the collecter voltage decreases which turns on Q3, allowing current to flow through R24. When Q2 is turned off, there is no current flow through R23; at this time, output is connected to ground. When the base of Q2 decreases to turn the transistor on, current flows through R23, developing a 3-volt level at the output, when 75 ohms termination is across R23. This level is set by R12, which establishes a constant current through Q1, set by U13-7.

Circuit configuration Q6, Q7, Q8, Q9, Q10, and U13-1 operates identically to the preceding circuit description.

The received ECL signals STA (J10), STB (J9), and RDA (J12), RDB (J11), and RTA (J14), RTB (J13) are connected through coaxial cables to the line receiver U1. Each group of signals has a 100 ohms termination (R52, R53, and R54) from line to line. The signals are received differentially and the true outputs U1-11, U1-13, and U1-9 are applied to multiplexer U11, pins 13, 21, and 1 respectively. When $\overline{\text{ECL}}$ at U6-11 is low, these outputs appear at Z_a, Z_b, and Z_c and connect to the GP031-1 receiver board, designated A6, via jacks J19, J20, and J21 (ST, RD, and RT respectively).

The received 50 Mbps TTL signals ST (J15), RD (J16), and RT (J17) are connected to ECL compatible comparators U3, U4, and U5. The reference U4-4 is set by the coltage divider R56 and R57 for 1.5V. When this level is exceeded, the output goes to an ECL high. When the $\overline{\text{TTL}}$ signal at U6-10 goes low, the gate output U6-12 goes high, selecting the TTL 50 Mbps inputs that appear at the Z_a, Z_b, and Z_c outputs.

The RS422 inputs are terminated with 100 ohms resistors R67, R68, and R69 applied to the RS422 receivers U8-5/6, U10-5/6, and U10-7/8. These receiver outputs are TTL compatible. A TTL to ECL translator U7 is necessary to convert the ECL levels into the multiplexer U11 input pins 15, 23, and 3. When the $\overline{\text{RS422}}$ signal at U6-6 goes low, the outputs U6-12 and U6-13 go high, transferring the RS422 signals to Z_a, Z_b, and Z_c. The RD output (Z_b) and RT output (Z_c) are fed to the GP031-1 board connectors JC and JD respectively (sheet 7 of logic diagram 500-0731). The differential ST output (Z_a and U4-12) is fed to the clock select and monitor circuit on the GP029-1 board (sheet 6 of logic diagram 500-0730).

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains the preventive and corrective maintenance procedures for the Model 607 DTTS. Maintenance procedures are relatively uncomplicated, due to the extensive use of integrated circuits.

Maintenance support data, in the form of diagrams, tables, and descriptive material, is provided in other sections of this manual. A functional block diagram and a discussion of the circuitry theory are presented in Section 4. Logic diagrams, assembly drawings, parts lists, and the chassis wiring list for the Model 607 DTTS are contained in Section 6. Information on the power supplies, CRT display monitor, frequency synthesizer, and the keyboard key switch assembly are contained in Appendices A, B, C, and D respectively.

The user should be thoroughly familiar with the Model 607 DTTS capabilities, theory of operation, and operating procedures before attempting any maintenance or troubleshooting procedures.

5.2 COMPONENT LOCATION

The physical location of the major components in the Model 607 DTTS chassis are shown in Figures 1-1 and 1-2, and in the assembly drawings in Section 6. The various subassembly components of the circuit boards, A1, A2, A4, A5, A6, A7, A9, are shown on the drawings in Section 6 and in the appendices (A8).

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance includes the performance of inspections which prevent or minimize downtime of the equipment. Through utilization of solid state circuitry, the checks and services are minimal. Table 5-1 shows the maintenance schedule for the Model 607. There are no components that require lubrication.

Table 5-1

Maintenance Schedule

NOMENCLATURE	TASK	INSPECTION FREQUENCY
Main Chassis	Check for excessive dirt, dust, or presence of foreign objects. Clean as required.	Monthly
Rack Slides	Check rack slides for ease of operation. Replace slide if bent, sticking, or otherwise damaged. Check for loose or misaligned hardware; tighten or realign as required.	3 Months
Internal Wiring and Wiring Harness	Check for frayed insulation, sharp bends, broken wires and faulty connections; repair or replace as required. Check for loose, damaged, or missing cable clamps; tighten or replace as required. Replace wiring or harness if other non-repairable defects are detected.	6 Months
Cooling Fan	Check for dust or dirt on or near fan. Clean as required. (This unit has sealed bearings and does not require lubrication.)	Monthly
DC Power Supplies	Check outputs of power supplies as described in paragraph 5.5.1.	Monthly

5.4 MINOR REPAIR REPLACEMENT

Minor repair procedures for the Model 607 DTTS are limited. Since the front panel power switch is a circuit breaker, there are no fuses to replace.

NOTE

If the circuit breaker constantly trips, determine cause of problem before replacement.

5.5 CORRECTIVE MAINTENANCE

Corrective maintenance of the Model 607 DTTS unit consists of repairs or adjustments, which must be made after malfunctions or failures occur, to restore the unit to normal operation. The corrective maintenance repairs should only be attempted by qualified personnel, knowledgeable in solid state logic and circuit theory, and, in particular, thoroughly familiar with the Model 607 DTTS theory of operation. Necessity for corrective maintenance is indicated, when any variation from the specified operational criteria of the unit is noted.

5.5.1 ADJUSTMENT PROCEDURES

There are two adjustments required for maintaining the Model 607 DTTS in proper working order: power supply voltage adjustments and TTL transmit data and clock driver adjustments.

5.5.1.1 Power Supplies. Two power supplies are utilized to provide the dc voltages required by the Model 607 circuitry. Power supply PS1, a Model DS 150-301 manufactured by digi-power, provides +5Vdc and ±12 Vdc; power supply PS2, a Model SK5-40/OVP manufactured by power-one INC., provides -5 Vdc. The chart below lists the actual voltages appearing at the board level.

Reference Designations	Board Type	Dc Voltages (±5%)
A1	Interface (INF014)	-2, -4.7, +5, +12
A2	Control Processor (PSR024)	-2, +5, ±12
A5	Transmitter (GP029)	-2, -4.7, +5
A6	Receiver (GP031)	-2, -4.7, +5
A7	Frequency Synthesizer	+12

These voltages should be checked, nominally on a monthly basis, to ensure that they are within a tolerance of ±5%. Convenient points to monitor -2V, +5V, and -4.7V are at hex standoffs V_{TT}, V_{CC}, and V_{EE} respectively at the edge of the GP029 transmitter board (A5). The ±12V can be checked at several points on the PSR024 board; e.g., IC DE31, pin 2 or 5 (-12V) and IC FA20, pin 4 or 8 (+12V). All voltages can be checked at terminal strips TB1 and TB2, which are accessible by removing the frequency synthesizer board (A7) and the INF014 interface board (A1). The chart below lists voltage and ground points at each of the TB1 and TB2 terminals.

TB1	Terminal	TB2
-4.7V	1	+5V
-4.7V	2	+5V
ECL GND	3	TTL to ECL GND
ECL GND	4	TTL GND
ECL GND	5	+12V
TTL to ECL GND	6	+12V
-2V	7	±12V GND
-2V	8	±12V GND
TTL GND	9	-12V

If a voltage is not within the specified ±5% tolerance, a power supply voltage adjustment is indicated. The power supply outline drawings in Appendix A illustrate the physical locations of the PS1 and PS2 voltage adjustment potentiometers. Note that of the voltages supplied by PS1 (±5V, ±12V), only +5V is adjustable. Also, the -2V requirement is obtained from the -5V source (PS2) via the emitter of transistor Q1, and only -5V (-4.7V at the board level) is directly adjustable. To gain access to the power supplies, raise the transmitter (A5) and receiver (A6) boards, and remove the control processor (A2) board.

5.5.1.2 TTL Interface Drivers. Adjustment to the interface board, needed for proper operation of the TTL interface drivers, is detailed in paragraph 3.3.4. The resistors to be adjusted are located directly behind the CRT assembly.

5.5.2 TROUBLESHOOTING PROCEDURES

Troubleshooting procedures should be performed in a logical sequence to isolate a malfunction to a specific location. Familiarization with the unit, which will enable the technical personnel to rapidly isolate the problem area, may be attained with the aid of the functional characteristics, circuit theory discussions, and logic and circuit diagrams presented elsewhere in this manual.

Malfunctions can generally be limited to one of seven major subassemblies: Interface board, A1 (INF014-1), Processor board, A2 (PSR024-2), CRT Display, A4, Transmitter board, A5 (GP029-1), Receiver board, A6, (GP031-1), Frequency Synthesizer board, A7 (SM-160), or Front Panel Keyboard, A8 (FPK001-1). Once isolated to a specific board, individual plug-in components can be monitored for correct waveforms by using a common "chip clip".

CAUTION

Do not measure the resistance of solid state devices. The device may be damaged by the application of voltages with improper polarities, or by the high short-circuit current of most volt-ohmmeters.

If normal operation of the unit indicates a malfunction, the following general items should be checked before beginning a troubleshooting procedure:

a. Power is applied to the unit (amber POWER indicator is lit). DC operating voltages are correct (-5 and +12 vdc).

b. All internal and external connectors are securely mated with the proper receptacles.

c. All required input signals are being received from the DCE.

d. All setup fields on the CRT are properly set for the particular function to be performed.

SECTION 6

DRAWINGS

6.1 GENERAL

This section contains the logic diagrams, schematics, assembly drawings, parts lists, and chassis wiring list for the Model 607 Data Transmission Test Set. Table 6-1 is a list of the assembly drawings, logic diagrams, schematics, parts lists, and the Model 607 Chassis Wire List. Table 6-2 is a list of the Manufacturer's Codes.

Table 6-1

Drawings and Parts Lists

Figure No.	Table No.	Page	Title	Drawing No.
6-1		6-9/ 6-10	Data Transmission Test Set Model 607, Chassis Assembly	355-0021-502
	6-3	6-13	Parts List, Data Transmission Test Set Model 607	-
6-2		6-19/ 6-20	Processor Card, Type PSR024-2, Assembly Drawing	460-1661-502
6-3		6-21	Component Board Assembly	300-0150-[ ]
6-3		6-22	Component Board Assembly AA1 (sheet 1)	300-0150-511
6-3		6-23	Component Board Assembly CA1 (sheet 2)	300-0150-501
6-3		6-24	Component Board Assembly DC31 (sheet 3)	300-0150-506
6-3		6-25	Component Board Assembly DG31 (sheet 4)	300-0150-507
6-3		6-26	Component Board Assembly EB31 (sheet 5)	300-0150-508
6-3		6-27	Component Board Assembly EH10 (sheet 6)	300-0150-504
6-3		6-28	Component Board Assembly EJ1 (sheet 7)	300-0150-502

Table 6-1

Drawings and Parts Lists (cont.)

Figure No.	Table No.	Page	Title	Drawing No.
6-3		6-29	Component Board Assembly FA10 (sheet 8)	300-0150-505
6-3		6-30	Component Board Assembly FC20 (sheet 9)	300-0150-510
	6-4	6-31	Parts List, PSR024-2 Circuit Card Assembly	-
6-4		6-45/ 6-46	Processor Card, Type PSR024-2, Logic Diagram	500-0712
6-5		6-67/ 6-68	Transmitter Card, Type GP029-1, Assembly Drawing	460-1660-501
	6-5	6-69	Parts List, GP029-1 Circuit Card Assembly	-
6-6		6-83/ 6-84	Transmitter Card, Type GP029-1, Logic Diagram	500-0730
6-7		6-115/ 6-116	Receiver Card, Type GP031-1, Assembly Drawing	460-1713-501
	6-6	6-117	Parts List, GP031-1 Circuit Card Assembly	
6-8		6-131/ 6-132	Receiver Card, Type GP031-1, Logic Diagram	500-0731
6-9		6-167/ 6-168	Interface Card, Type INF014-1, Assembly and Schematic Diagram	460-1658-501
	6-7	6-173	Parts List, INF014-1 Circuit Card Assembly	-
6-10		6-183/ 6-184	Front Panel Keyboard Card, Type FPK001-1, Assembly Drawing	460-1678-501
	6-8	6-185	Parts List, FPK001-1 Circuit Card Assembly	-
6-11		6-187/ 6-188	Unit Code Card Assembly and Parts List	460-1547-501
6-12		6-189	Model 607 Chassis Wire List	730-1998

Table 6-2

MANUFACTURERS' CODES

Code	Manufacturer
00779	AMP, Inc. P. O. Box 3608 Harrisburg, PA 17105
01295	Texas Instruments, Inc. Semiconductor Group P. O. Box 5012 13500 North Central Expressway Dallas, TX 73222
04713	Motorola, Inc. Semiconductor Products Division P. O. Box 20923 5005 E. McDowell Road Phoenix, AZ 85036
05245	Corcam Inc. 2635 N. Kildare Ave. Chicago, IL 60639
05828	General Inst. Corp. Gov. Systems Div. 600 W. John St. Hicksville, NY 11802
07047	Ross Milton Co. 511 Second St. Pike Southampton, PA 18966
07263	Fairchild Camera and Instrument Corp. Semiconductor Division 464 Ellis St. Mountain View, CA 94042
07413	Protospec 420 South Date Alhambia, CA 91803
09022	Cornell-Dubilier Electric Corp. Mica Div. Providence, RI

Table 6-2

MANUFACTURERS' CODES (cont.)

Code	Manufacturer
09022	Pacific Electric Co. 1605 Rodney French Blvd. New Bedford, MA 02741
13103	Thermalloy Co., Inc. 2021 W. Valley View Lane P. O. Box 340839 Dallas, TX 75234
14949	Trompeter Electronics, Inc. 8936 Comanche Ave. Chatsworth, CA 91311
19112	Garry Mfg. Co. 1010 Jersey Ave. New Brunswick, NJ 08902
20747	Aydin Monitor Systems 502 Office Center Dr. Fort Washington, PA 19034
23936	Pamotor 770 Airport Blvd. Burlingame, CA 94010
27014	National Semiconductor Corp. 2900 Semiconductor Drive Santa Clara, CA 95051
27802	Vectron Laboratories Inc. 166 Glover Ave. Norwalk, CT 06850
29587	Bunker Ramo Corp. Amphenol Industrial Division 1830 S. 54th Ave. Chicago, IL 60650
30194	Component Enterprises Co., Inc. 235-275 E. Penn St. P. O. Box 189 Norristown, PA 19404

Table 6-2

MANUFACTURERS' CODES (cont.)

Code	Manufacturer
31433	Union Carbide Corp., Electronics Div. Highway 276 SE P. O. Box 5928 Greenville, SC 29606
34335	Advanced Micro Devices 901 Thompson Pl. Sunnyvale, CA 94086
34649	Intel Corp. 3065 Bowers Ave. Santa Clara, CA 95051
54407	Power-One Inc. 740 Calle Plano Dr. Camarillo, CA 93010
54776	Syntest Corp. 169 Milham St. Marlboro, MA 01752
56289	Sprague Electric Company North Adams, MA 01247
56708	Zilog Inc. 10460 Bubb Road Cupertino, CA 95014
71279	Cambridge Thermionic Corp. 445 Concord Ave. Cambridge, MA 02138
71450	CTS Corp. 905 N. West Blvd. Elkhart, IN 46514
71468	ITT Cannon Electric 666 E. Dyer Road Santa Ana, CA 92705
71590	Globe-Union Inc. Centralab Electronics Div. Highway 20 W. P. O. Box 858 Fort Dodge, IA 50501

Table 6-2

MANUFACTURERS' CODES (cont.)

Code	Manufacturer
71785	TRW Cinch Connectors 1501 Morse Ave. Elk Grove Village, IL 60007
72259	Nytronics Inc. 105 Madison Ave. New York, NY 10016
73138	Beckman Instruments, Inc. Hilipot Division 2500 Harbor Blvd. Fullerton, CA 92634
75037	Minnesota Mining and Mfg. Co. Electro Products Division 3M Center St. Paul, MN 55101
75382	Kulka Electric Corp. 633-643 S. Fulton Ave. Mt. Vernon, NY 10550
80294	Bourns, Inc. Instrument Division 6135 Magnolia Ave. Riverside, CA 92506
81349	Military Specifications Promulgated By Military Departments/Agencies Under Authority of Defense Standardization Manual 4120 3-M
81541	Airpax Electronics Inc. Woods Road Cambridge, MA 21613
83508	Grant Pulley and Hardware Co. High Street West Nyack, NY 10994
91506	Augat, Inc. 33 Perry Ave. Attleboro, MA 02703

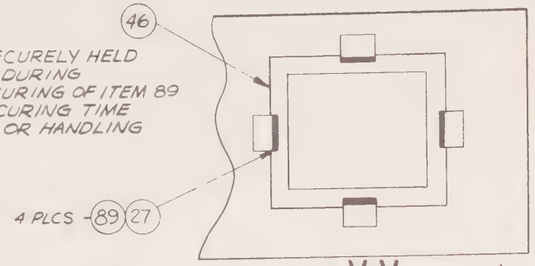
Table 6-2

MANUFACTURERS' CODES (cont.)

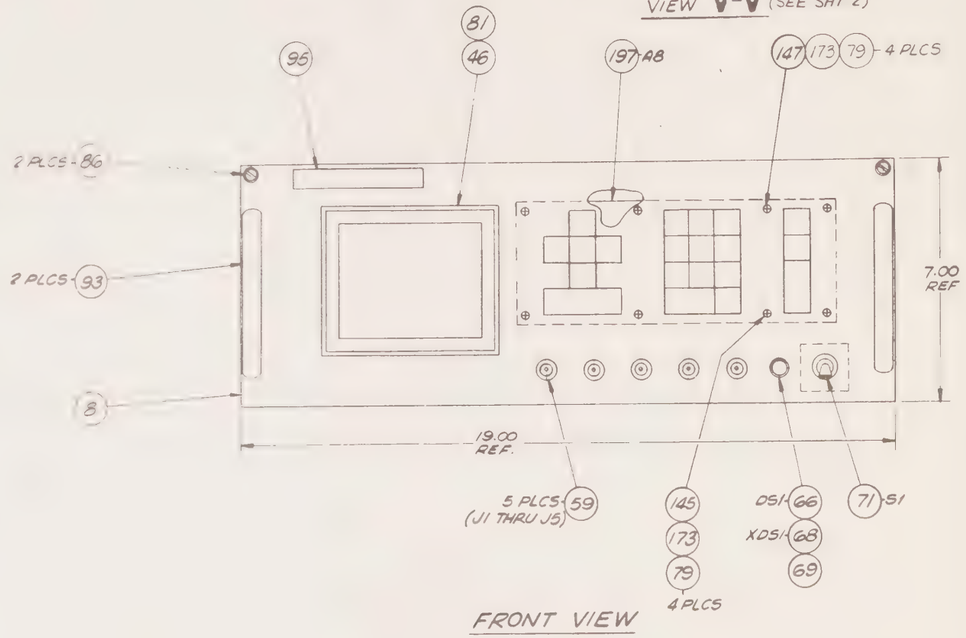
Code	Manufacturer
91929	Honeywell Inc. Micro Switch Division 11 W. Spring St. Freeport, IL 61032
95348	Gordos Corp. 250 Glenwood Ave. Bloomfield, NJ 07033
96906	Military Standards
98291	Selecto Corp. 225 Hoyt Namaroneck, NY 10544
98978	International Electronic Research Corp. 135 W. Magnolia Blvd. Burbank, CA 91502

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 05166		
	C	REVISED PER ECO 05844	5 DEC 1980	
	D	REVISED PER ECO 06144		
	E	REVISED PER ECO 06128	3 APR 1981	
	F	REVISED PER ECO 06625	26 AUG 81	
	G	REVISED PER ECO 06640	26 AUG 81	
	H	REVISED PER ECO 06719	26 AUG 81	
	J	REVISED PER ECO 07045 KRM 22 DEC 81		

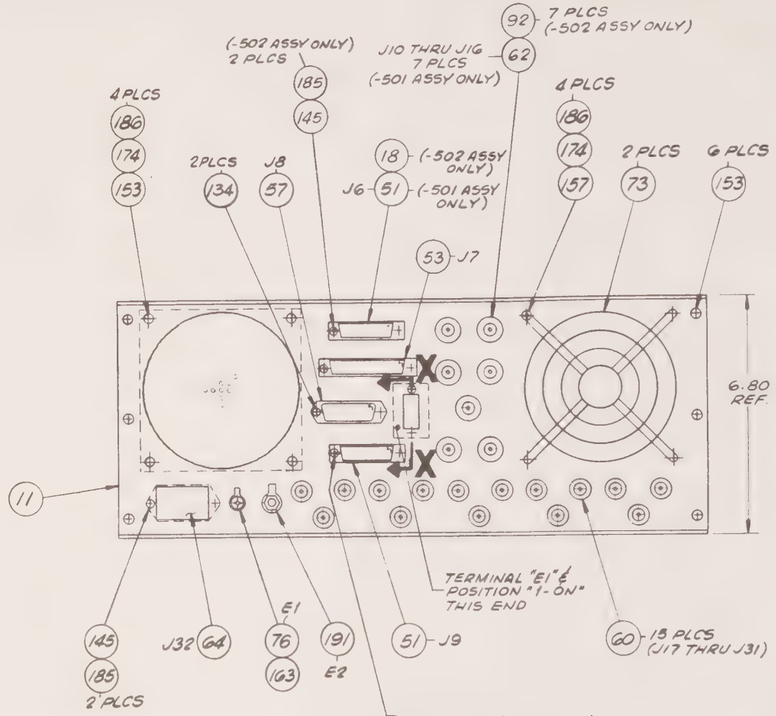
NOTE:
ITEM 46 TO BE SECURELY HELD AGAINST ITEM 8 DURING APPLICATION & CURING OF ITEM 89
ALLOW 4 HOURS CURING TIME BEFORE MOVING OR HANDLING FINISHED ASSY



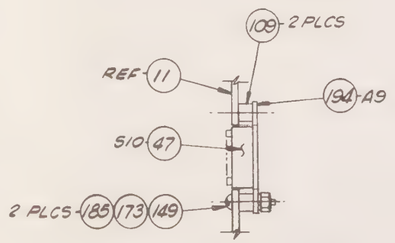
VIEW V-V (SEE SHT 2)



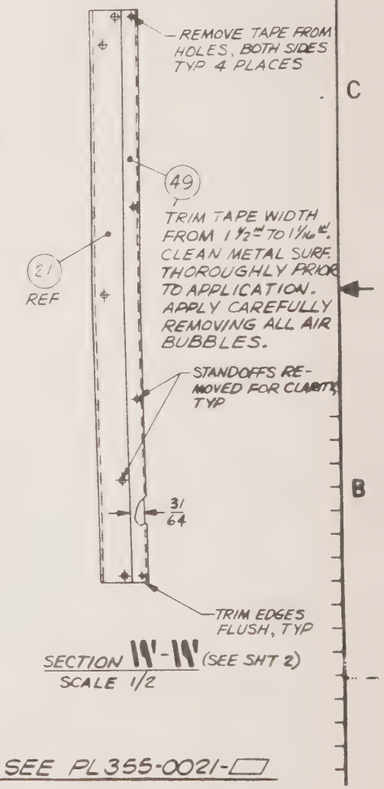
FRONT VIEW



REAR VIEW



SECTION X-X
SCALE : FULL



SECTION W-W (SEE SHT 2)
SCALE 1/2

FOR PARTS LIST SEE PL355-0021-☐

800-0684-1

Figure 6-1. Model 607 Data Transmission Test Set Chassis Assembly (sheet 1)

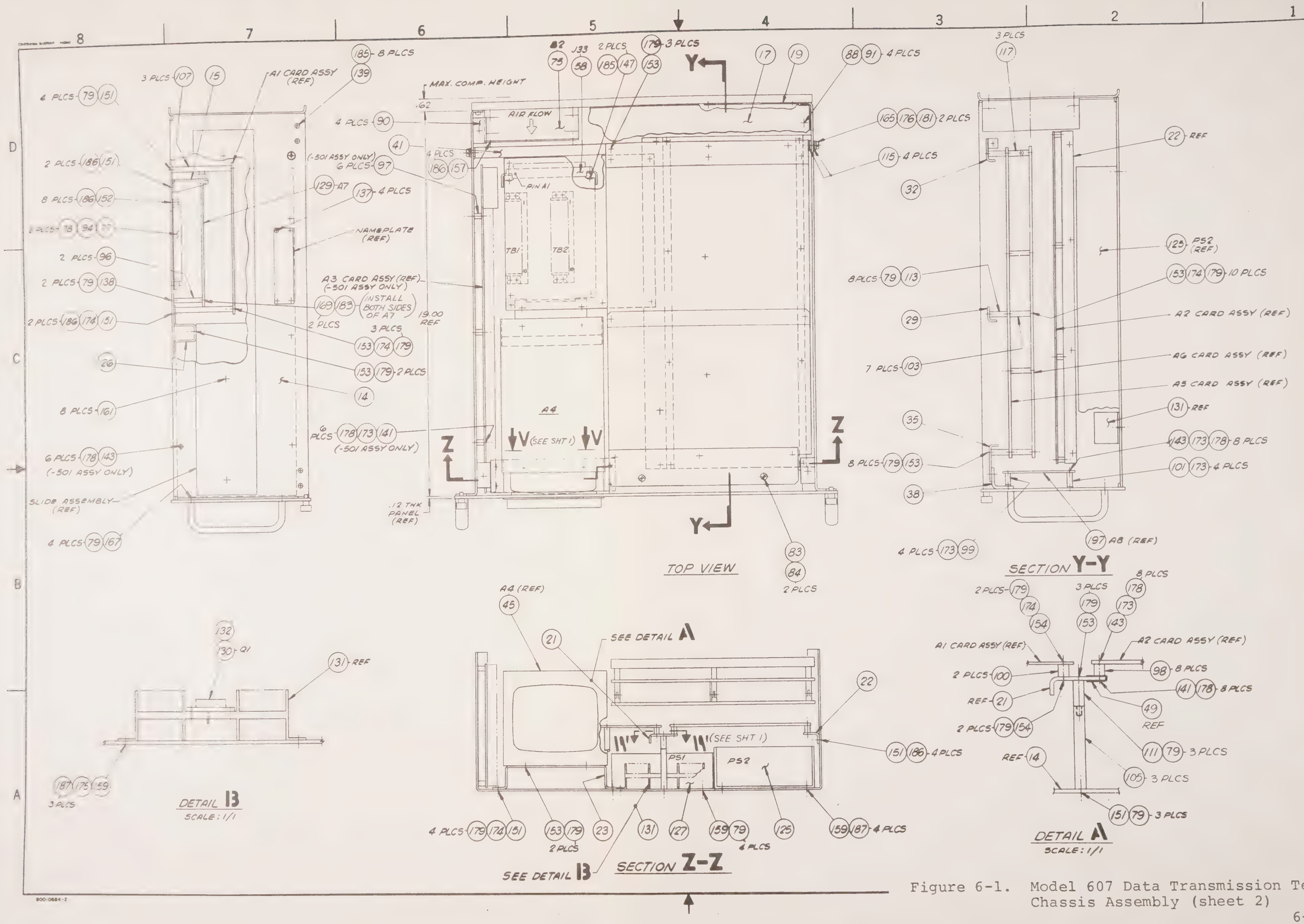


Figure 6-1. Model 607 Data Transmission Test Set Chassis Assembly (sheet 2)

Table 6-3

Parts List, Data Transmission Test Set Model 607

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		DATA TRANSMISSION TEST SET MODEL 607 CHASSIS ASSY.	20747	355-0021-502	REF
A1	6-1	Circuit Card Assy., INFO14-1 (See Table 6-7 for Parts Breakdown)	20747	460-1658-501	1
A1P1-A1P6		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	16
A1P7, A1P8		Connector, Coaxial 75 ohm RT Angle Plug	98291	50-111-9511	5
A1P9,A1P10		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	REF
A1P11,A1P12		Connector, Coaxial 50 ohm RT Angle Plug	98291	50-311-3188	4
A1P13,A1P14		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	REF
A1P15-A1P17		Connector, Coaxial 75 ohm RT Angle Plug	98291	50-111-9511	REF
A1P18		Not Used			
A1P20,A1P21		Connector, Coaxial 50 ohm RT Angle Plug	98291	50-311-3188	REF
A2	6-1	Circuit Card Assy., PSR024-2 (See Table 6-4 for Parts Breakdown)	20747	460-1661-502	1
A2FD43	6-12	Connector, DIP 16 Pin Plug	75037	3416-0000	14
A2PA,$\overline{\text{A2PA}}$, $\overline{\text{A2PB}}$,A2PC, A2PD,$\overline{\text{A2PD}}$, A2PE,$\overline{\text{A2PE}}$, A2PF,$\overline{\text{A2PF}}$	6-12	Connector, DIP 16 Pin Plug	75037	3416-0000	REF

Table 6-3

Parts List, Data Transmission Test Set Model 607 (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
A3		Not Used			
A4	6-1	CRT Data Display, 5 Inch (See Appendix for Parts Breakdown)	Audio-tronics	DC-946-31	1
A4P1		Connector, 10 Pin Card Edge	71785	250-10-30-170	1
A5		Circuit Card Assy., GPO29-1 (See Table 6-5 for Parts Breakdown)	20747	460-1660-501	1
A5PA,A5PB		Connector, 50 Pin Card Edge Plug	75037	3425-6050	4
A5PC,A5PD, A5PE		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	REF
A5PINN		Connector, DIP 14 Pin Plug	75037	3406-0000	3
A5P5X		Connector, DIP 16 Pin Cable Terminator	71279	702-1023-01-00-00	7
A5P7HH		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	REF
A5P12E		Connector, DIP 14 Pin Plug	75037	3406-0000	REF
A5P13B		Connector, DIP 16 Pin Plug	75037	3416-0000	REF
A6		Circuit Card Assy., GPO31-1 (See Table 6-6 for Parts Breakdown)	20747	460-1713-501	1
A6PA,A6PB		Connector, 50 Pin Card Edge Plug	75037	3425-6050	REF
A6PC,A6PD		Connector, Coaxial 50 ohm Plug	98291	50-007-0000	REF
A6PINN	6-1	Connector, DIP 14 Pin Plug	75037	3406-0000	REF

Table 6-3

Parts List, Data Transmission Test Set Model 607 (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
A6P5X	6-1	Connector, DIP 16 Pin Cable Terminator	71279	702-1023-01-00-00	REF
A7		Module, Frequency Synthesizer (See Appendix for Parts Breakdown)	54776	SM-160	1
A7P1		Connector, Coax SMA Plug	30194	SMA-M-15A	1
A8		Circuit Card Assy., FPK001-1 (See Table 6-8 for Parts Breakdown)	29747	460-1678-501	1
A8P1,A8P2		Connector, DIP 16 Pin Plug	75037	3416-0000	REF
A9		Printed Wiring Board	20747	400-611	1
B1		Not Used			
B2		Fan, Cooling 115 VAC 50/60 HZ 110 CFM	23936	4600X	1
J1 - J5		Connector, Coax BNC	14949	BJ-27	5
J6,J9		Connector, 25 Pin Receptacle Screwlock, Female	71468 71468	DB-25S D20418-2	2 4
J7		Connector, 37 Pin Receptacle Screwlock, Female	71468 71468	DC-37S D20418-2	1 2
J8		Connector, 24 Pin Receptacle	29587	57-20240-2	1
J10-J16	6-1	Not Used Button Plug	83058	SS-51142-K2915	7

Table 6-3

Parts List, Data Transmission Test Set Model 607 (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
J17 - J31	6-1	Connector, Coax BNC Feed-Thru	14949	BJ-28	15
J32		Connector, Power Line/RFI	05245	3EF1	1
J33		Connector, 22 Pin Double Readout	71785	251-22-30-160	1
P17 - P26		Connector, BNC Plug	00779	2-330061-1	10
P27 - P31		Connector, BNC Plug	00779	2-329544-1	5
PS1		Power Supply, 3 Output +12 v @ 4A, -12v @ 1A, +5v @24 (See Appendix for Parts Breakdown)	Digital Power Corp.	DS150-301	1
PS2		Power Supply, 5V @ 40 Amp (See Appendix for Parts Breakdown)	54407	SK5-40/OVP	1
Q1		Transistor, Silicon PNP Heatsink, TO-3	04713 13103	2N6377 6401B-2	1 1
R1		Resistor, Fxd. Composition 100 Ohms, ±5%, 1/2 WATT	81349	RC20GF101J	1
S1		Circuit Breaker, Double Pole 2 Amp	81541	T21-2-5.00A-01-20LS	1
S2 - S9		Not Used			
S10		Switch, 8 Position SPST DIP	00779	435166-5	1
TB1, TB2	6-1	Terminal Block, 10 Position Jumper, Terminal Strip Marker Strip, 10 Posit Terminal Board	75382 75382 75382	600A-10 600J MS600-10-XP-4C	2 9 2

Table 6-3

Parts List, Data Transmission Test Set Model 607 (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
XDS1	6-1	Lampholder, Indicator	96906	LH74/1	1
		Lens, Amber	96906	LC13YN2	1
		Lamp, Neon	96906	MS25252-C7A	1

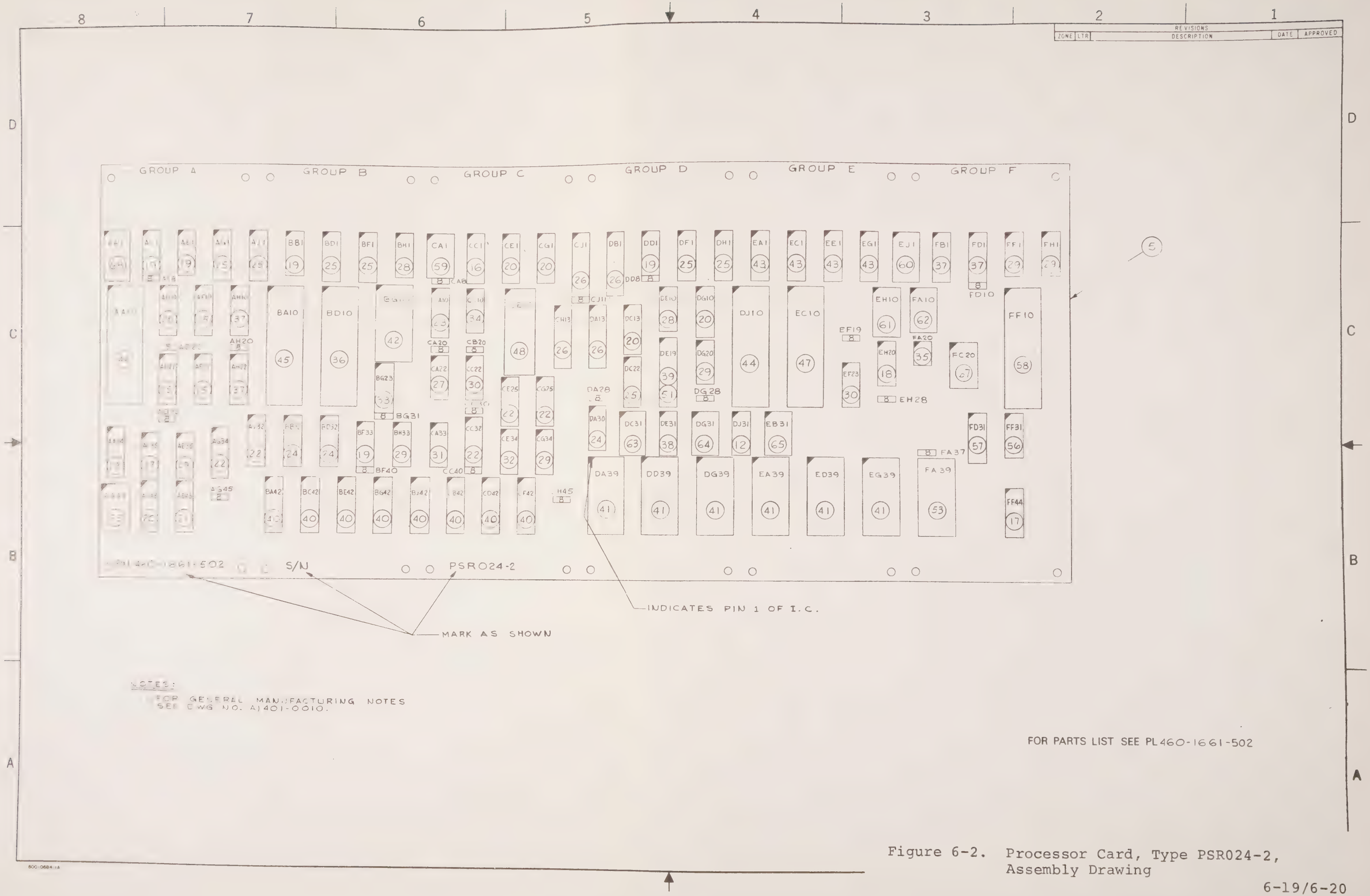


Figure 6-2. Processor Card, Type PSR024-2, Assembly Drawing

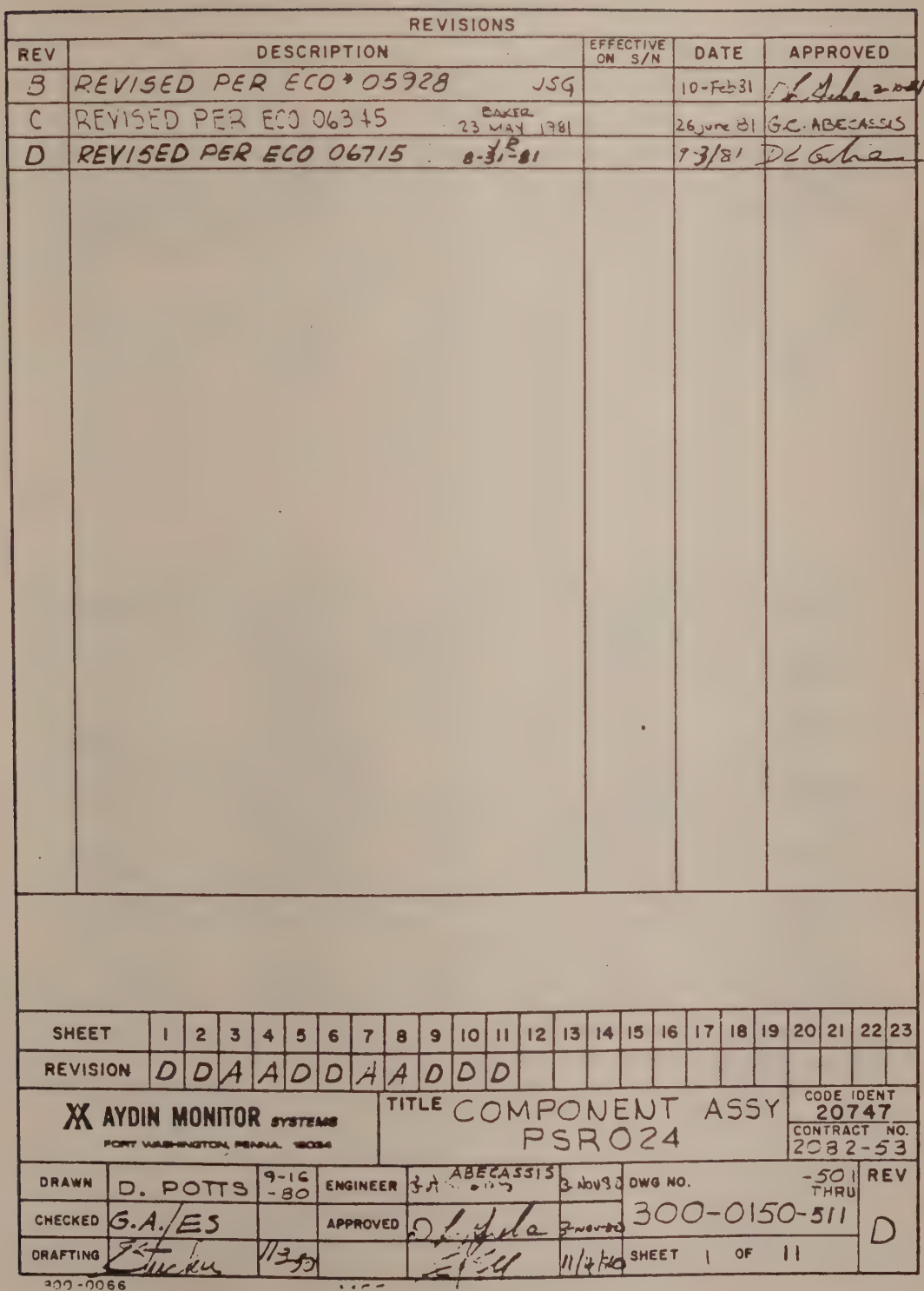


Figure 6-3. Component Board Assembly

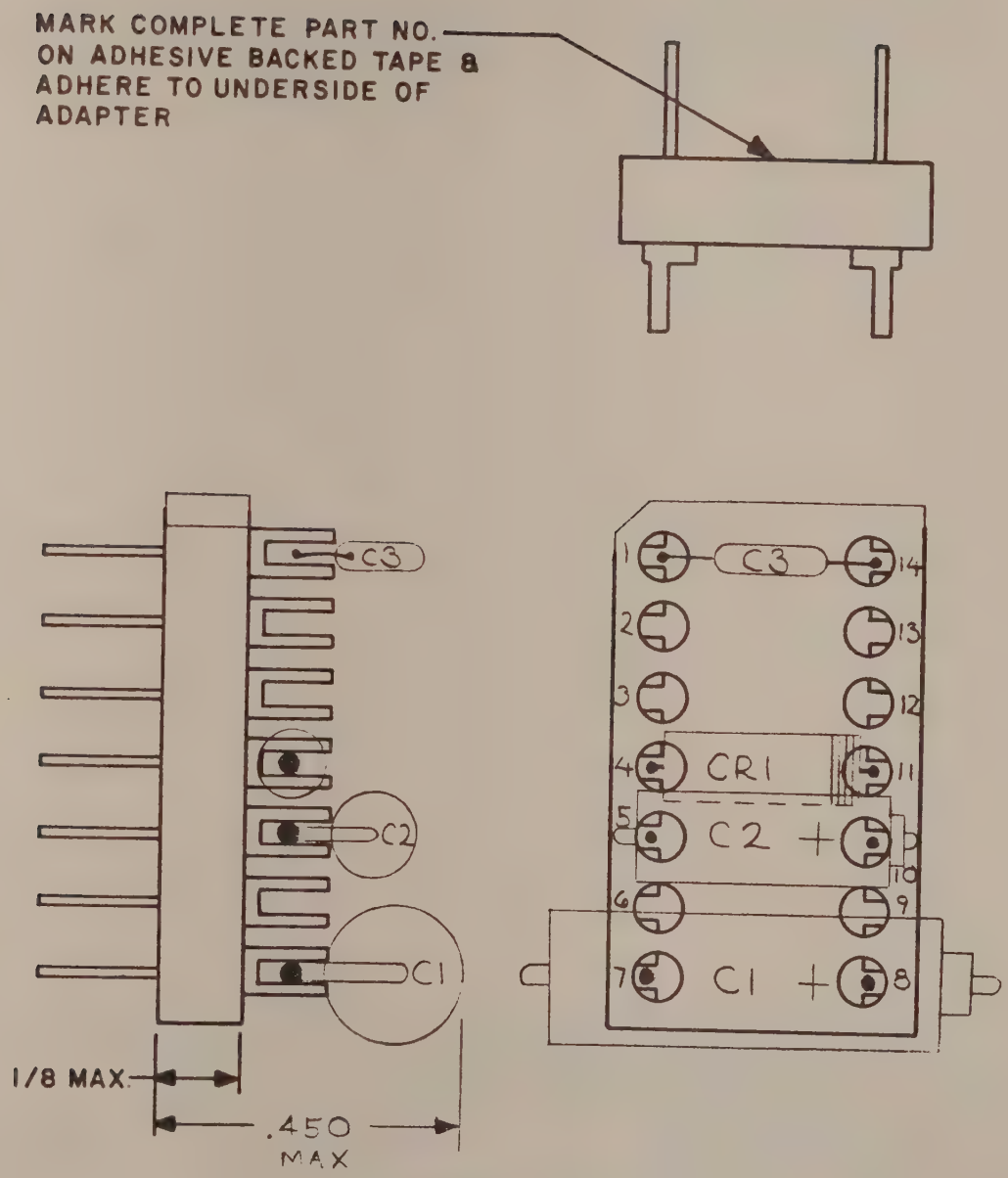


Figure 6-3. Component Board Assembly AA1 (sheet 1)

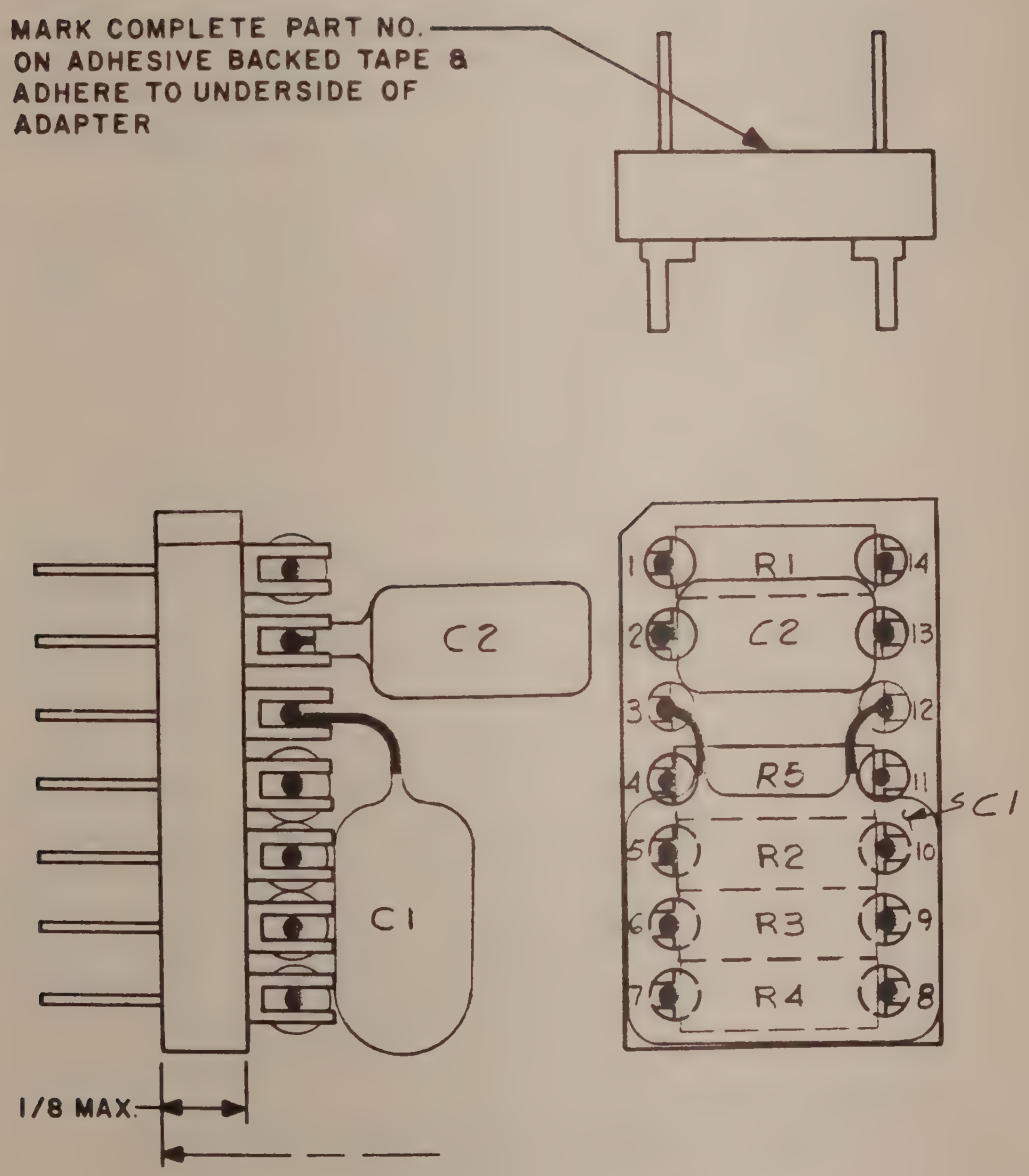


Figure 6-3. Component Board Assembly CA1 (sheet 2)

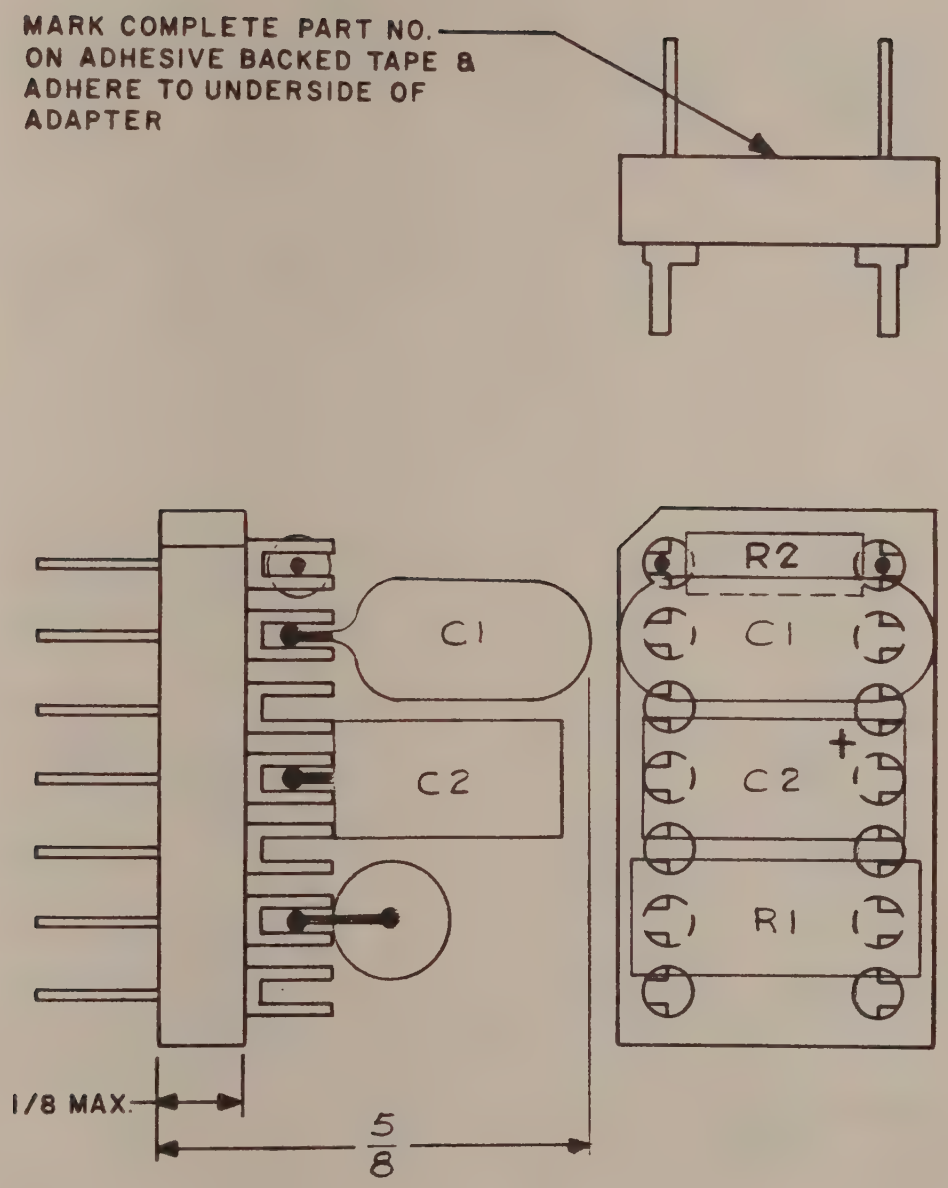


Figure 6-3. Component Board Assembly DC31 (sheet 3)

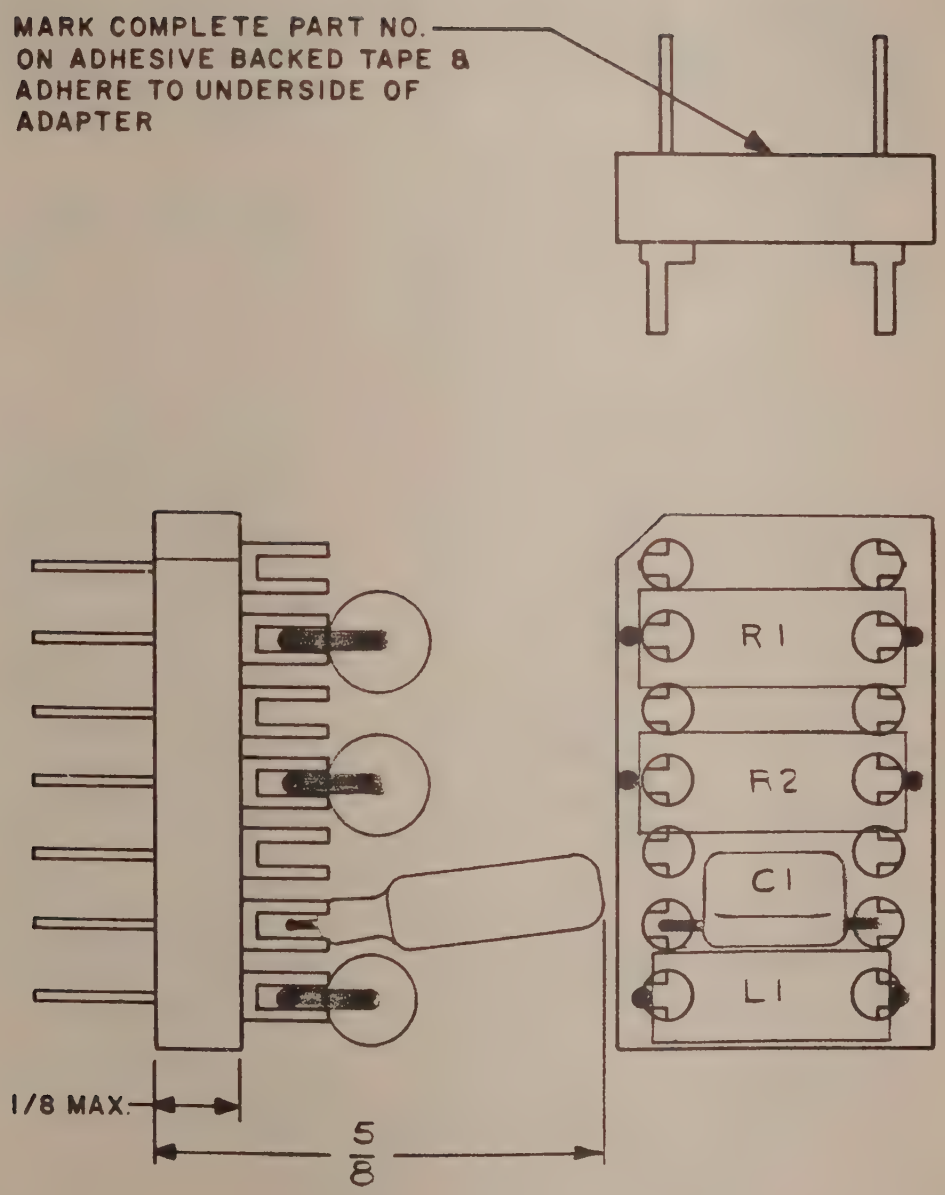


Figure 6-3. Component Board Assembly DG31 (sheet 4)

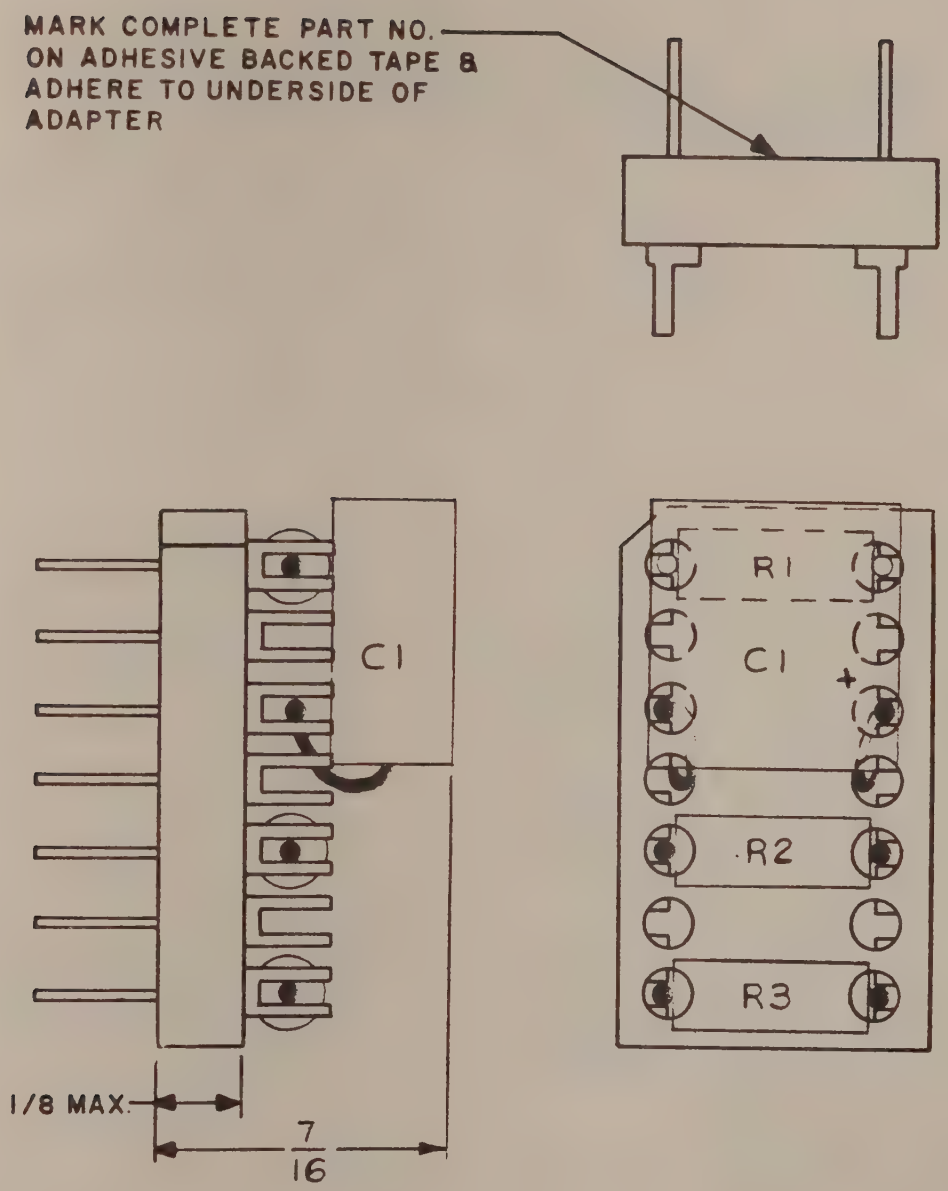


Figure 6-3. Component Board Assembly EB31 (sheet 5)

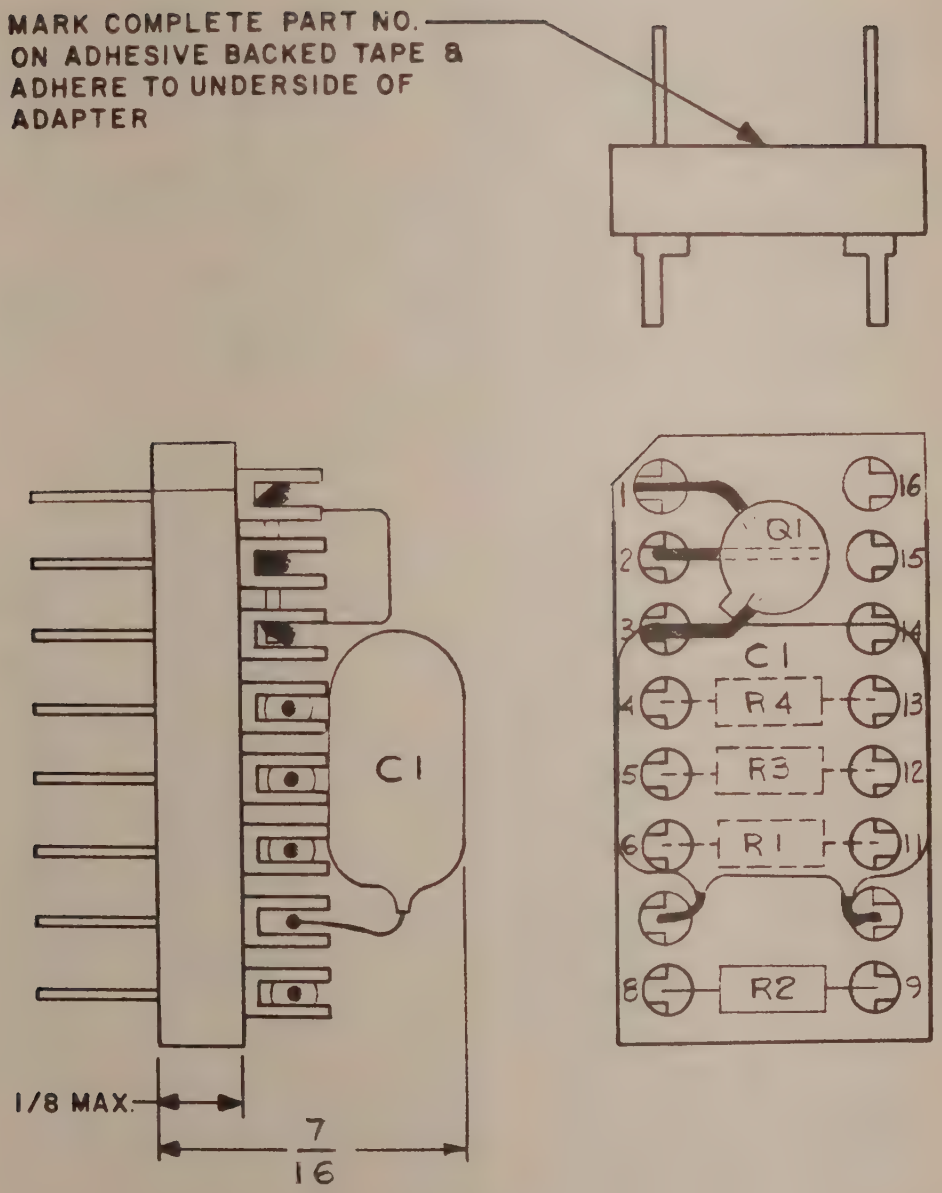


Figure 6-3. Component Board Assembly EH10 (sheet 6)

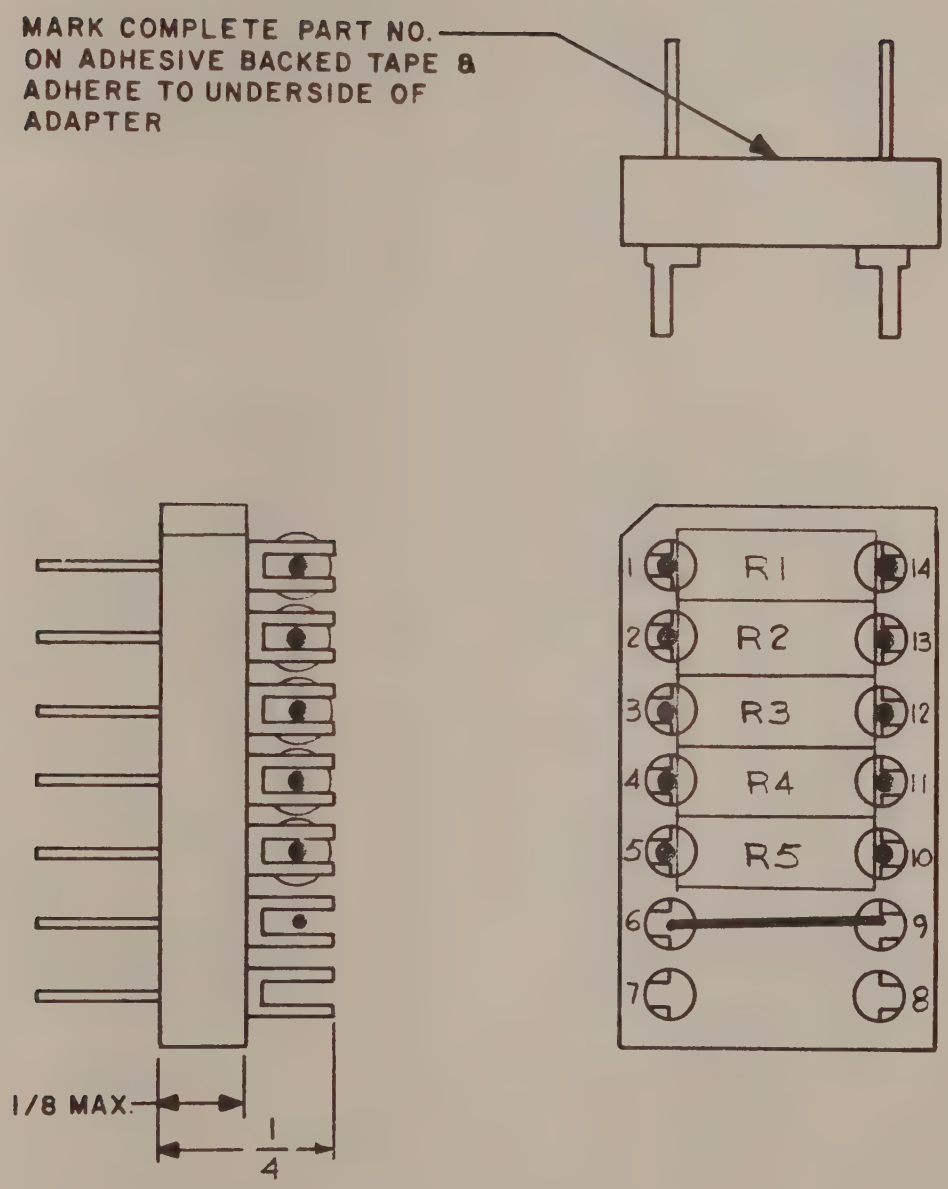


Figure 6-3. Component Board Assembly EJ1 (sheet 7)

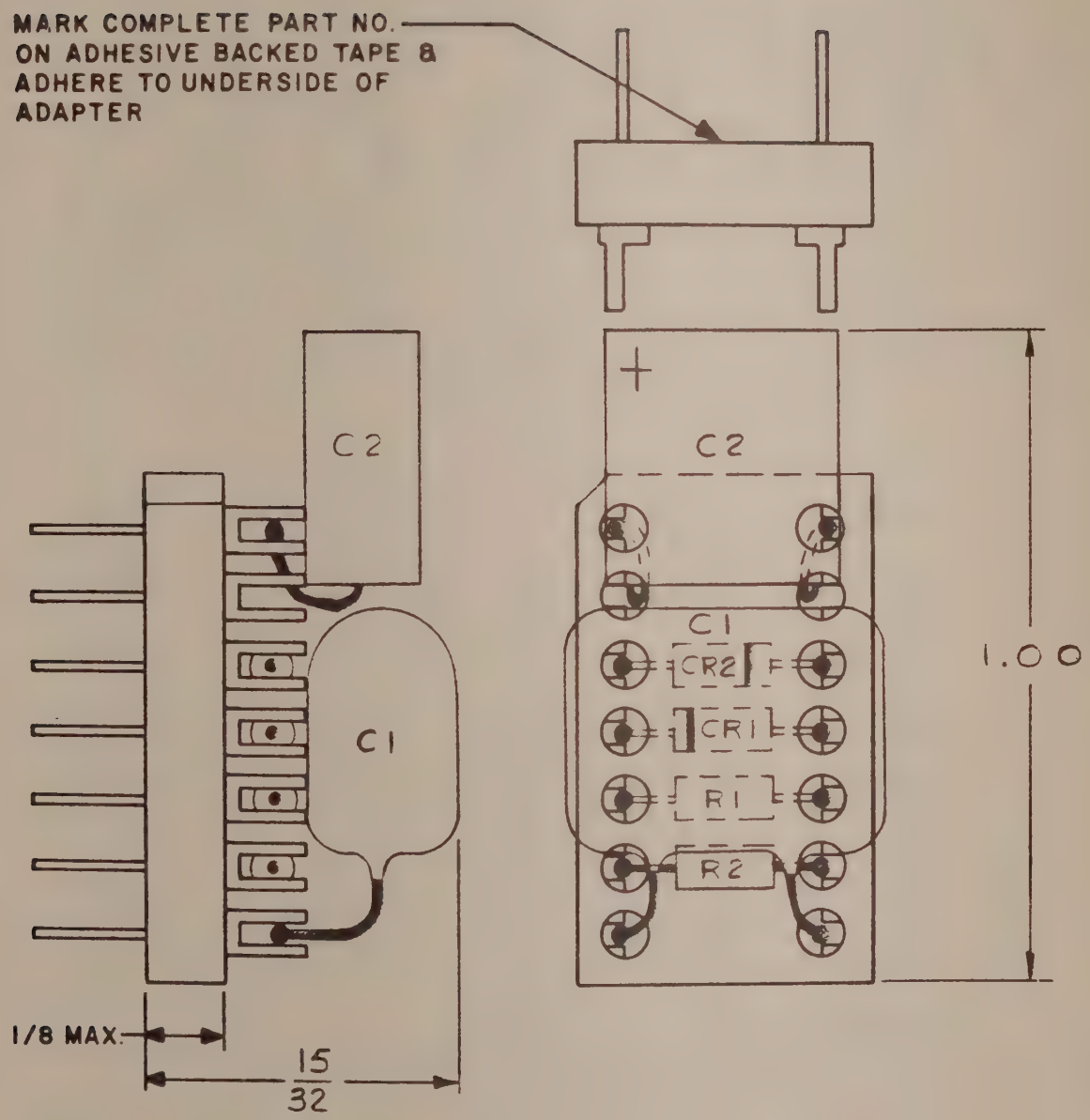


Figure 6-3. Component Board Assembly FA10 (sheet 8)

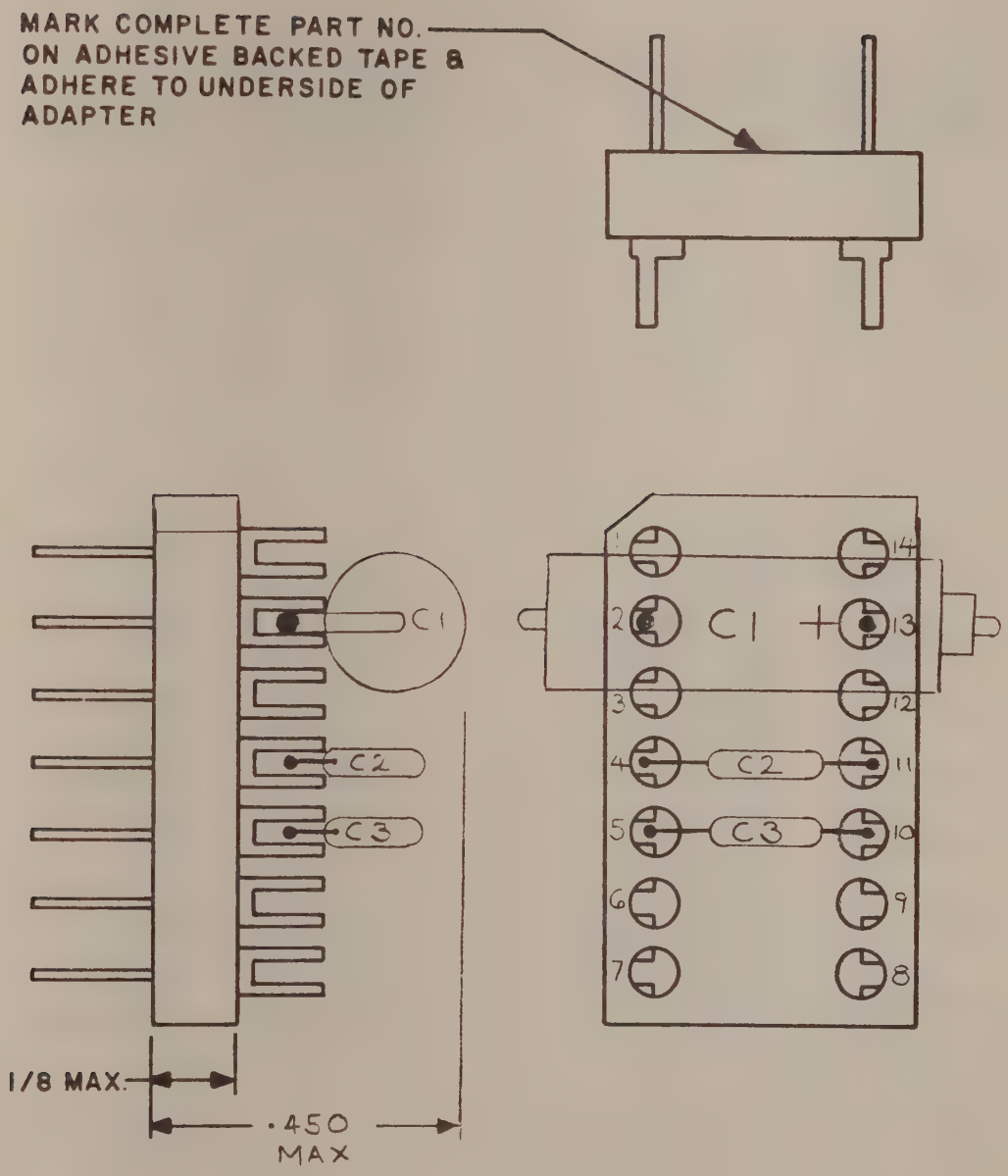


Figure 6-3. Component Board Assembly FC20 (sheet 9)

Table 6-4

Parts List, PSR024-2 Circuit Card Assy.

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		CIRCUIT CARD ASSY., PSR024-2	20747	460-1661-502	REF
AA1	6-2	Component Board Assy.	20747	300-0150-511	1
C1	6-3	Capacitor, Fxd. Tantalum 6.8 uf, ±10%, 35 Vdcw	56289	150D685X903582	1
C2	6-3	Capacitor, Fxd. Tantalum 2.2 uf, ±20%, 20 Vdcw	56289	150D225X0020A2	1
C3	6-3	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 100 Vdcw	71590	CY30A104M	1
CR1	6-3	Diode, Silicon	04713	1N914	1
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
AA10	6-2	Central Processing Unit, 8-Bit	56708	8400ZP00S	1
AA34	6-2	Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	6
AA44	6-2	Oscillator, Crystal Clock 18.432 MHZ	27802	C0-238A-6 (18.432 MHZ)	1
AC1	6-2	Resistor Array, DIP 13 4.7K, ±2%, 0.15 WATT	73138	899-1-R4.7K	5
AC8	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	21
AC35	6-2	Integrated Circuit 2-Input Positive NAND Gate	01295	SN74LS00N-10	2

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
AC43	6-2	Integrated Circuit 3 to 8 Line Decoder/Multiplexer	01295	SN74LS138N-10	5
AD10		Integrated Circuit Bus Driver	01295	SN74LS367N-10	11
AD20		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
AD22		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
AD32		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
AE1		Resistor Array, DIP 13 4.7K, ±2%, 0.15 WATT	73138	899-1-R4.7K	REF
AE35		Integrated Circuit Inverter	01295	SN74LS04N-10	6
AE43		Integrated Circuit 2 to 4 Line Decoder/Multiplexer	01295	SN74LS139N-10	1
AF10, AF22, AG1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
AG34		Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	REF
AG35		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
AH10	6-2	Integrated Circuit Parallel Bidirectional Bus Driver	34649	P8216	4

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
AH20	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
AH22		Integrated Circuit Parallel Bidirectional Bus Driver	34649	P8216	REF
AJ1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
AJ32		Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	REF
BA10		Integrated Circuit 2-Port Direct Memory Access	56708	8410ZC00S	1
BA42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	8
BB1		Resistor Array, DIP 13 4.7K, ±2%, 0.15 WATT	73138	899-1-R4.7K	REF
BB32		Integrated Circuit 4-Bit Bidirectional Shift Register	01295	SN74LS194N-10	3
BC42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
BD1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
BD10		Integrated Circuit Programmable CRT Controller	34649	P8275	1
BD32	6-2	Integrated Circuit 4-Bit Bidirectional Shift Register	01295	SN74LS194N-10	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
BE42	6-2	Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
BF1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
BF33		Resistor Array, DIP 13 4.7K, ±2%, 0.15 WATT	73138	899-1-R4.7K	REF
BF40		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
BG10		Integrated Circuit 8912 Bit Read Only Memory	04713	MCM66750P	1
BG23		Integrated Circuit 4-Bit Binary Full Adder	01295	SN74LS83N-10	1
BG31		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
BG42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
BH1		Integrated Circuit 2-Input Positive NOR gate	01295	SN74LS02N-10	2
BH33		Integrated Circuit Inverter	01295	SN74LS04N-10	REF
BJ42	6-2	Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
CA1	6-2	Component Board Assy.	20747	300-0150-501	1
C1	6-3	Capacitor, Fxd. Mica 100 pf, ±5%, 500 Vdcw	09022	CD15FD101J03	1
C2		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 100 Vdcw	71590	CY30A104M	1
R1		Resistor, Fxd. Composition 15K, ±5%, 1/4 WATT	81349	RC07GF153J	1
R2 - R4		Resistor, Fxd. Composition 4.7K, ±5%, 1/4 WATT	81349	RC07GF472J	3
R5	6-3	Resistor, Fxd. Composition 6.2K, ±5%, 1/4 WATT	81349	RC07GF622J	1
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
CA8	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CA10		Integrated Circuit 8-Bit Shift Register	01295	SN74LS166N-10	1
CA20		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CA22		Integrated Circuit 2-Input Positive NAND Gate	01295	SN74LS00N-10	REF
CA33	6-2	Integrated Circuit Positive NAND Gate	01295	SN74LS20N-10	1

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
CB20	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CB42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
CC1		Integrated Circuit Monostable Multivibrator	01295	SN74LS221N-10	1
CC10		Integrated Circuit 2-Input Exclusive OR Gate	01295	SN74LS86N-10	1
CC22		Integrated Circuit 2-Input Positive AND Gate	01295	SN74LS08N-10	2
CC30		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CC32		Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	REF
CC40		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CD42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
CE1		Integrated Circuit 3-8 Line Decoder/Multiplexer	01295	SN74LS138N-10	REF
CE10		Integrated Circuit 4-Channel Counter Timer	56708	8430ZC00S	1
CE25	6-2	Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
CE34	6-2	Integrated Circuit D Type Flip-Flop	01295	SN74LS74N-10	1
CF42		Integrated Circuit 1024 x 4 Bit Static RAM	34649	P2114A-4	REF
CG1		Integrated Circuit 3-8 Line Decoder/Multiplexer	01295	SN74LS138N-10	REF
CG25		Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS163N-10	REF
CG34		Integrated Circuit Inverter	01295	SN74LS04N-10	REF
CH13		Integrated Circuit D Type Flip-Flop	01295	SN74LS374N-10	4
CH45		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
CJ1		Integrated Circuit D Type Flip-Flop	01295	SN74LS374N-10	REF
CJ11		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
DA13		Integrated Circuit D Type Flip-Flop	01295	SN74LS374N-10	REF
DA28	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
DA30	6-2	Integrated Circuit 4-Bit Bidirectional Shift Register	01295	SN74LS194N-10	REF
DA39		Integrated Circuit 16K Erasable PROM, Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0080	1
DB1		Integrated Circuit D Type Flip-Flop	01295	SN74LS374N-10	REF
DC13		Integrated Circuit 3-8 Line Decoder/Multiplexer	01295	SN74LS138N-10	REF
DC22		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
DC31	6-2	Component Assy.	20747	300-0150-506	1
C1	6-3	Capacitor, Fxd. MICA 39 pf, ±5%, 500 Vdcw	09022	CD15ED390J03	1
C2		Capacitor, Fxd. Tantalum 6.8 uf, ±20%, 35 Vdcw	31433	T330C685M035AS	1
R1		Resistor, Fxd. Composition 3.3 Ohms, ±5%, 1/2 WATT	81349	RC20GF3R3J	1
R2	6-3	Resistor, Fxd. Composition 1K, ±5%, 1/4 WATT	81349	RC07GF102J	1
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
DD1	6-2	Resistor Array, DIP 13 4.7K, ±2%, 0.15 WATT	73138	899-1-R4.7K	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
DD8	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
DD39		Integrated Circuit 16K Erasable PROM, Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0081	1
DE10		Integrated Circuit 2-Input Positive NOR Gate	01295	SN74LS02N-10	REF
DE19		Plug, Adapter LS1/4K	19112	622-4KR	1
DE19		Integrated Circuit 4096 High Speed ROM	05828	ER3400	1
DE31		Integrated Circuit Voltage Regulator	01295	TL497ACN	1
DF1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
DG10		Integrated Circuit 3 to 8 Line Decoder/Multiplexer	01295	SN74LS138N-10	REF
DG20		Integrated Circuit Inverter	01295	SN74LS04N-10	REF
DG28		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
DG31	6-2	Component Assy.	20747	300-0150-507	1
C1	6-3	Capacitor, Fxd. Ceramic 1.0 uf, ±20%, 50 Vdcw	71590	CY30C105M	1

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
L1	6-3	Inductor, 220 uh	72259	WEE-WEE-220	1
R1	6-3	Resistor, Fxd. Composition 16K, ±5%, 1/2 WATT	81349	RC20GF163J	1
R2	6-3	Resistor, Fxd. Composition 1.2K, ±5%, 1/2 WATT	81349	RC20GF122J	1
DG39	6-2	Integrated Circuit 16K Erasable PROM Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0082	1
DH1		Integrated Circuit Bus Driver	01295	SN74LS367N-10	REF
DJ10		Integrated Circuit GPIB Talker/Listener	34649	P8291	1
DJ31		Relay, DIP Reed 1 Form C	95348	GB835C-2	1
EA1		Integrated Circuit 3-State Bus Transceiver	04713	MC3448AP	4
EA39		Integrated Circuit 16K Erasable PROM, Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0083	1
EB31	6-2	Component Assy.	20747	300-0150-508	1
C1	6-3	Capacitor, Fxd. Tantalum 6.8 uf, ±20%, 35 Vdcw	31433	T330C685M035AS	1
R1	6-3	Resistor, Fxd. Composition 220 Ohms, ±5%, 1/4 WATT	81349	RC07GF221J	1
R2, R3	6-3	Resistor, Fxd. Composition 4.7K, ±5%, 1/4 WATT	81349	RC07GF472J	2

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
EC1	6-2	Integrated Circuit 3-State Bus Transceiver	04713	MC3448AP	REF
EC10		Integrated Circuit 2-Port Parallel I/O	56708	8420ZC00S	1
ED39		Integrated Circuit 16K Erasable PROM, Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0084	1
EE1		Integrated Circuit 3-State Bus Transceiver	04713	MC3448AP	REF
EF19		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
EF23		Integrated Circuit 2-Input Positive AND Gate	01295	SN74LS08N-10	REF
EG1		Integrated Circuit 3-State Bus Transceiver	04713	MC3448AP	REF
EG39		Integrated Circuit 16K Erasable PROM, Mfr. 34649, Mfr. P/N D2716-1 (unprogrammed)	20747	291-0085	1
EH10	6-2	Component Assy.	20747	300-0150-504	1
C1	6-3	Capacitor, Fxd. MICA 100 pf, ±5%, 500 Vdcw	09022	CD15FD101J03	1
Q1	6-3	Transistor, Silicon PNP	04713	2N2907	1

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R1	6-3	Resistor, Fxd. Film 2K, ±1%, 1/8 WATT	81349	RN55D2001F	1
R2	6-3	Resistor, Fxd. Film 5.11K, ±1%, 1/8 WATT	81349	RN55D5111F	1
R3,R4	6-3	Resistor, Fxd. Composition 1K, ±5%, 1/8 WATT	81349	RC05GF102J	2
EH20	6-2	Integrated Circuit Voltage Regulator	04713	MC1723CL	1
EH28	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CZ5U104P050B	REF
EJ1	6-2	Component Assy.	20747	300-0150-502	1
R1,R3	6-3	Resistor, Fxd. Composition 220 Ohms, ±5%, 1/4 WATT	81349	RC07GF221J	2
R2,R4	6-3	Resistor, Fxd. Composition 330 Ohms, ±5%, 1/4 WATT	81349	RC07GF331J	2
R5	6-3	Resistor, Fxd. Composition 1K, ±5%, 1/4 WATT	81349	RC07GF102J	1
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
FA10	6-2	Component Assy.	20747	300-0150-505	1
C1	6-3	Capacitor, Fxd. MICA 1000 pf, ±5%, 100 Vdcw	09022	CD15CA102J03	1
C2	6-3	Capacitor, Fxd. Tantalum 10 uf, ±20%, 35 Vdcw	31433	T330C106M035AS	1
CR1, CR2	6-3	Diode, Silicon	04713	1N914	2

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R1	6-3	Resistor, Fxd. Composition 2K, ±5%, 1/8 WATT	81349	RC05GF202J	1
R2	6-3	Resistor, Fxd. Composition 6.8K, ±5%, 1/8 WATT	81349	RC05GF682J	1
		Plug, 14 Pin DIP Adapter	91506	614-CG1	1
FA20	6-2	Integrated Circuit, Timer	27014	LM555CN	1
FA37	6-2	Capacitor, Fxd. Ceramic	56289	923CZ5U104P050B	REF
FA39	|	Integrated Circuit 32K Erasable PROM, Mfr. 34649, Mfr. P/N P2732A (unprogrammed)	20747	291-0095	1
FB1	6-2	Integrated Circuit Bidirectional Bus Driver	34649	P8216	REF
FC20	6-2	Component Assy.	20747	300-0150-510	1
C1	6-3	Capacitor, Fxd. Tantalum 6.8 uf, ±10%, 35 Vdcw	56289	150D685X9035B2	1
C2,C3	6-3	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 100 Vdcw	71590	CY30A104M	2
		Plug, 14 Pin DIP Adapter			
FD1	6-2	Integrated Circuit Bidirectional Bus Driver	34649	P8216	REF
FD10	6-2	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	56289	923CX5U104P050B	REF
FD31	6-2	Integrated Circuit RS-232C Line Receiver	04713	MC1489AL	1
FF1,FH1	6-2	Integrated Circuit, Inverter	01295	SN74LS04N-10	REF

Table 6-4

Parts List, PSR024-2 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
FF10	6-2	Integrated Circuit, Serial Input/Output Controller	56708	84402PAOS	1
FF31	6-2	Integrated Circuit RS-232C Line Driver	04713	MC1488L	1
FF44	6-2	Integrated Circuit Synchronous 4-Bit Counter	01295	SN74LS393N-10	1
	6-2	Modular Board, Universal	19112	NCS23-054-15-3BSNC	1

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 07586 CHT 4-23-83	6-13-83	
	C	REVISED PER ECO 08084 JSG		
	D	REVISED PER ECO 08269	3-3-83	
	E	REVISED PER ECO 08341 JS 4-4-83	4-7-83	
	F	REVISED PER ECO 08371 DD 4-7-83	4-11-83	
	G	REVISED PER ECO 08632 DD 8-8-83	8-12-83	

(1)AC35-8 DB READ

8216 AH10 — DB0(H) DB1(H) DB2(H) DB3(H) — (3)(4)(5)(6)(7)(8)(9)(10)(11)

8216 AH22 — DB4(H) DB5(H) DB6(H) DB7(H) — (3)(4)(5)(6)(7)(8)(9)(10)(11)

Z80A — D0 D1 D2 D3 D4 D5 D6 D7; A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11; INT WAIT NMI BUSREQ RESET CLK; IORQ RD WR RFSH HALT BUSACK; MREQ M1

(3)(6)(7) INT(L)
(9)CE34-06 WAIT(L)
(6)BA10-15 BUSRQ(L)

AA1 — AC1 4.7K ×4

AA44 — CO-238A-6 18.432MHZ

AA34 — 74LS163A

12 MHZ(H)
2.3 MHZ(H) (3)(6)(7)(9)
4.6 MHZ(H)
9.3 MHZ(H)
18.432 MHZ (H) (6)
RESET(H) (7)
RESET(L) (3)(7)

AC35 — 74LS00; AE35 — 74LS04; IN 914 CR1; 2.2μf C2

74LS367 AD10 — A0 A1 A2 A3 A4 A5 → AB00(H) AB01(H) AB02(H) AB03(H) AB04(H) AB05(H)

74LS367 AF10 — A6 A7 A8 A9 A10 A11 → AB06(H) AB07(H) AB08(H) AB09(H) AB10(H) AB11(H)

74LS367 AD22 — A12 A13 A14 A15 MREQ M1 → AB12(H) AB13(H) AB14(H) AB15(H) MRQ(L) MI(L)

74LS367 AF22 — IORQ RD WR RFSH HALT BUSACK → RD(H) IORQ(L) RD(L) WR(L) RFSH(L) BUSACK(L) BUSACK(H)

74LS04 AE35 — RD(H)

COMP ASSY DC31 — +5 1K R2 — PUP (2)(7)(9)

74LS02 DE10; 74LS04 DG20; 74LS00 AC35 — DB READ (1)

MICROPROCESSOR

Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 1)

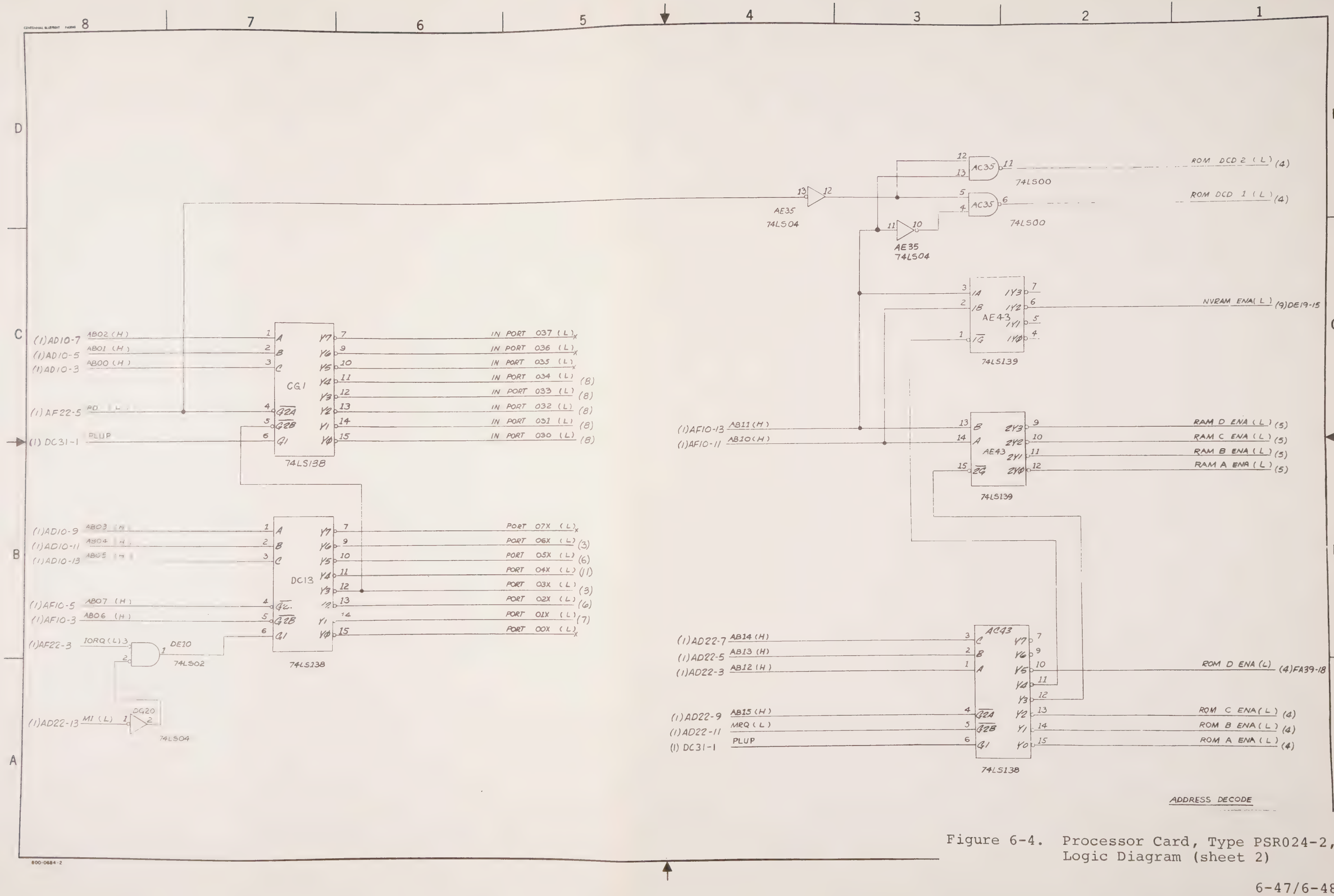


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 2)

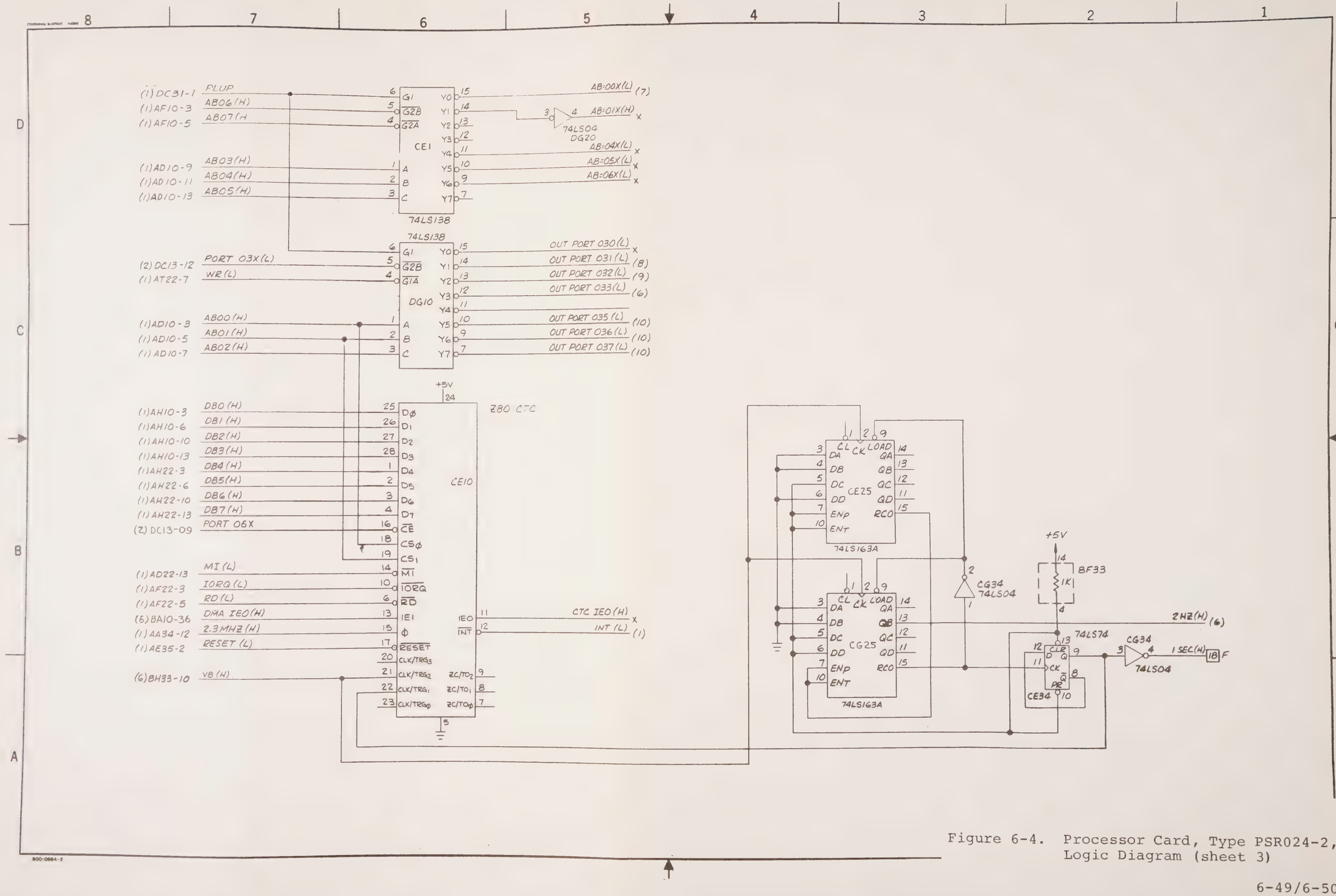


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 3)

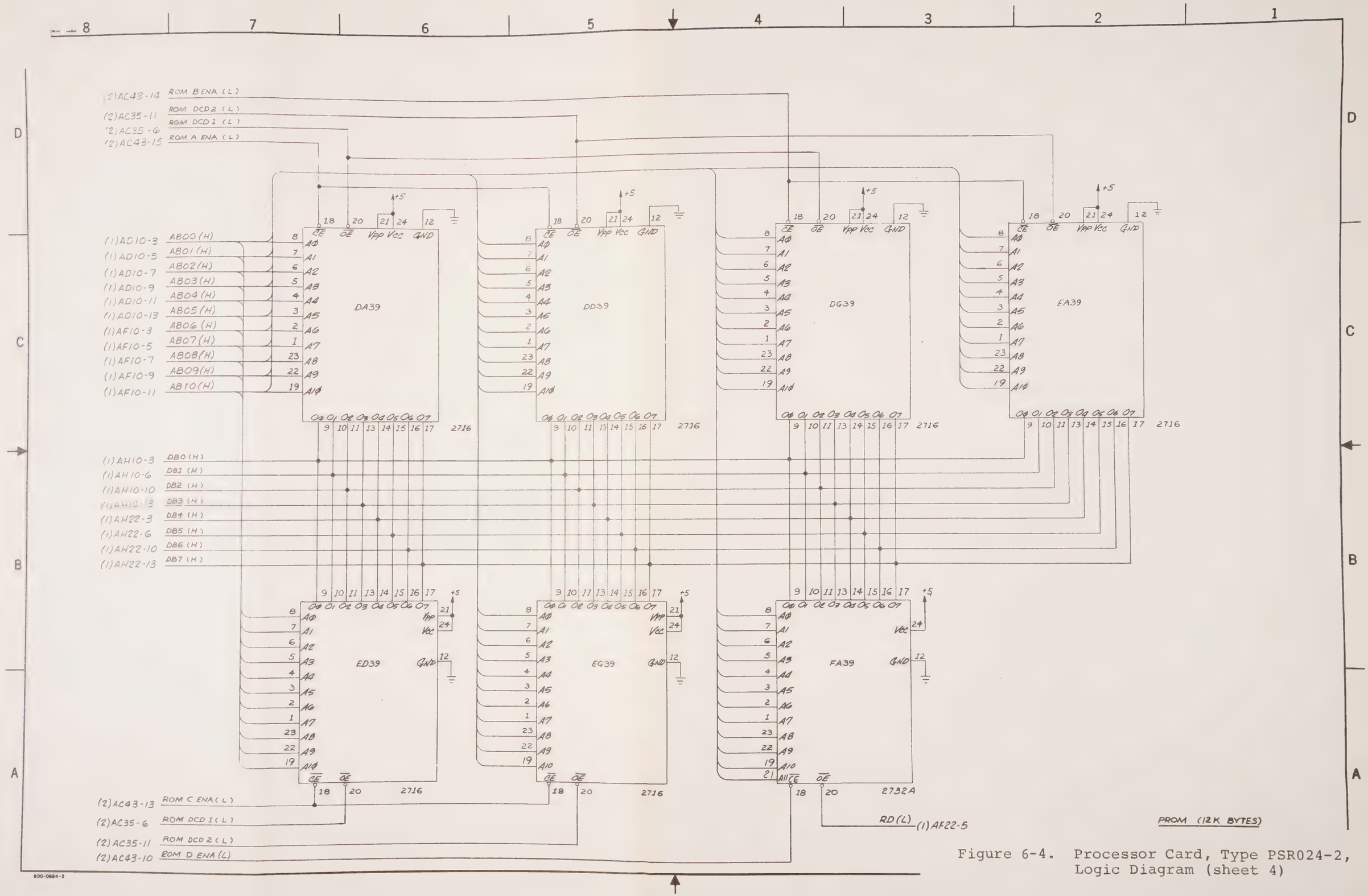


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 4)

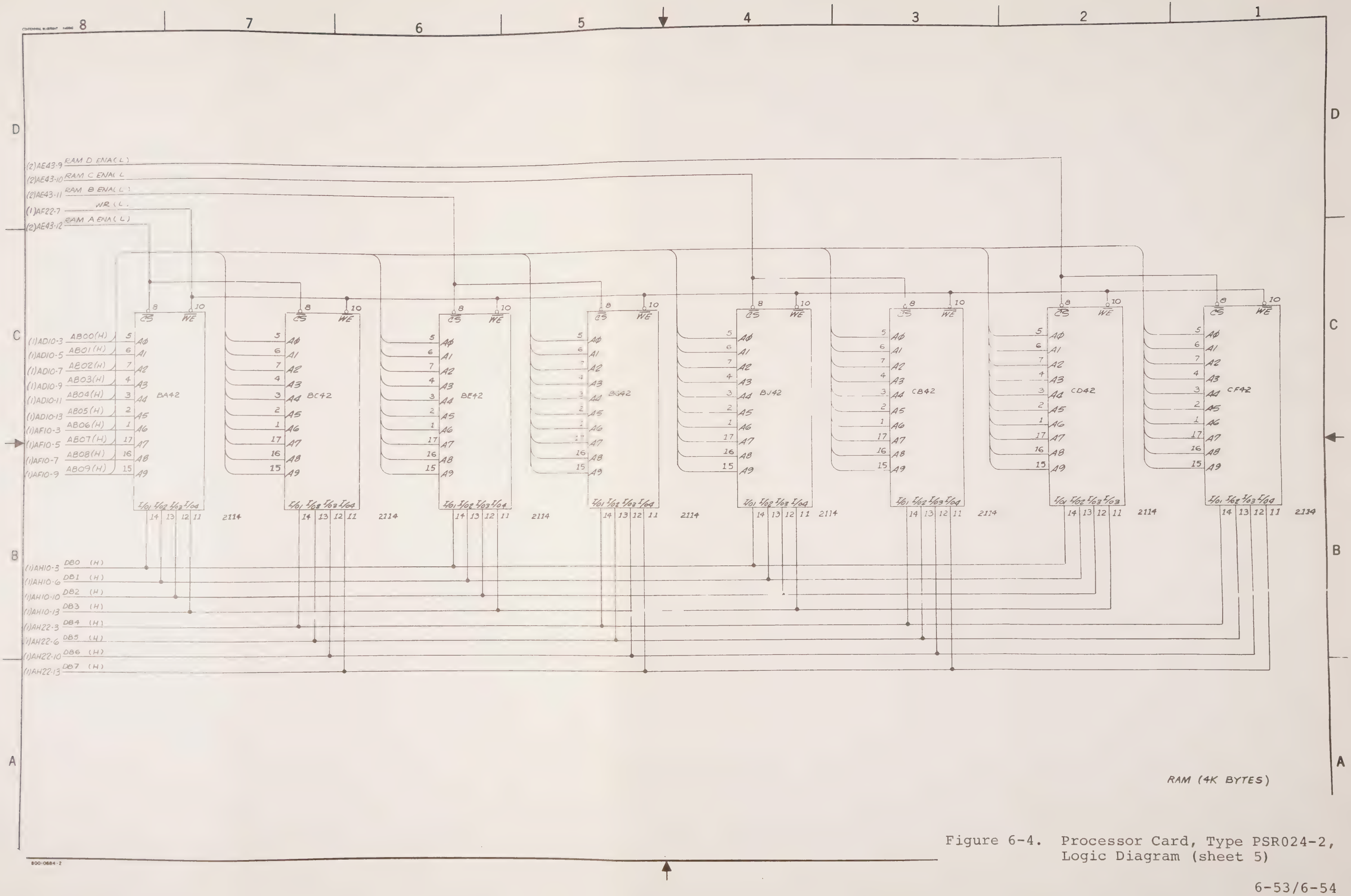


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 5)

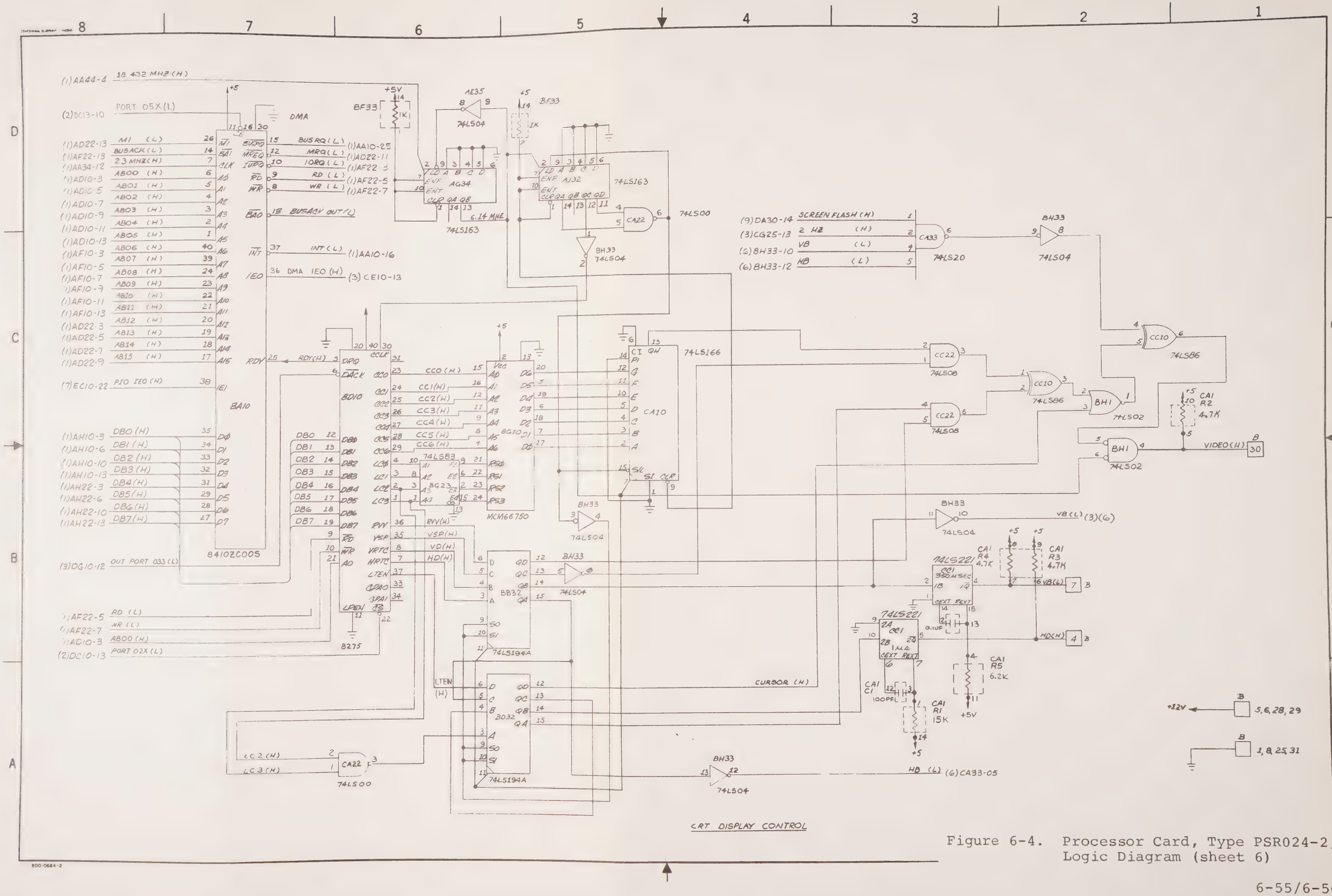


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 6)

PARALLEL INTERFACE (ECL, 488) CONTROL

Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 7)

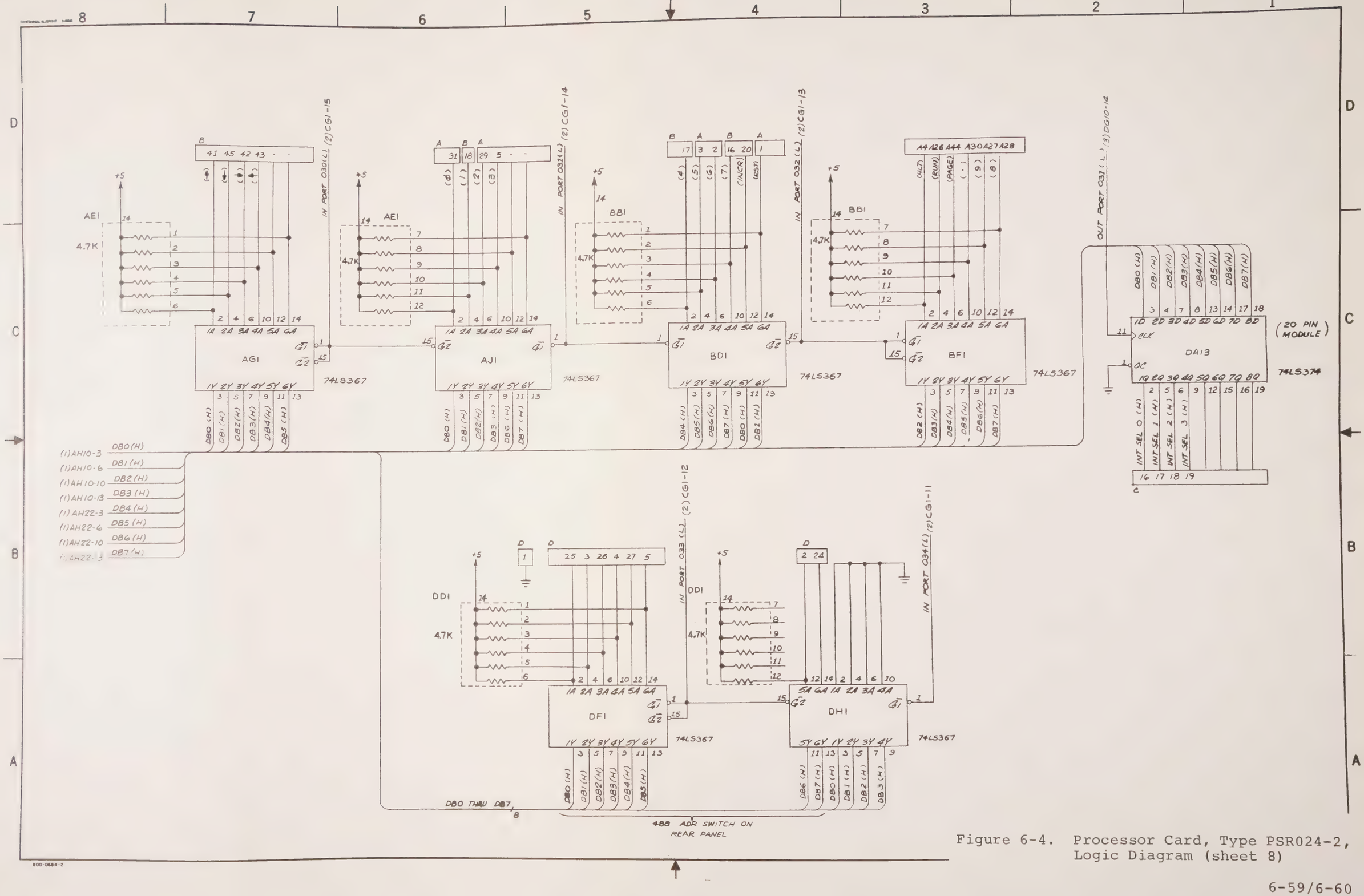
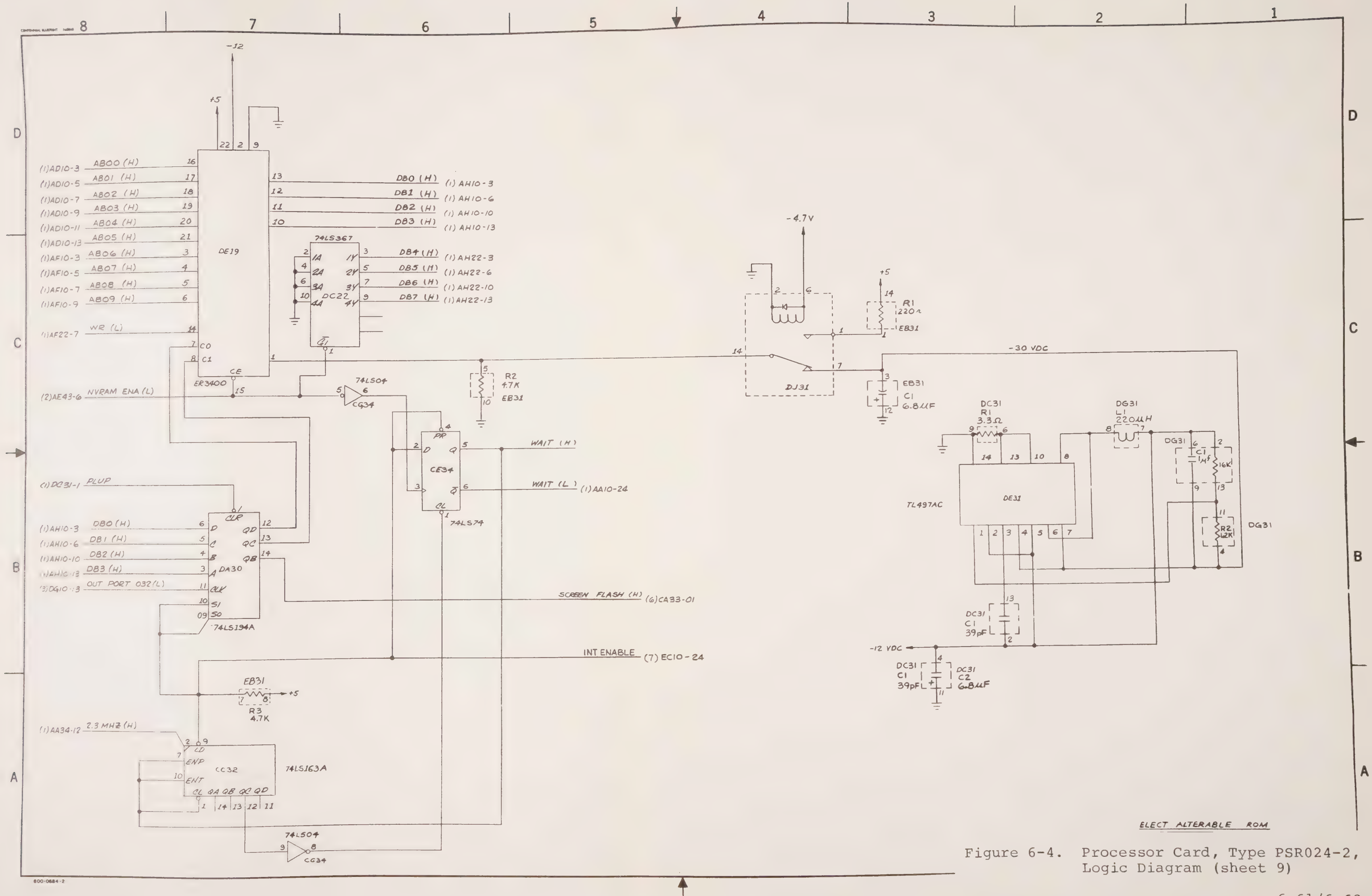


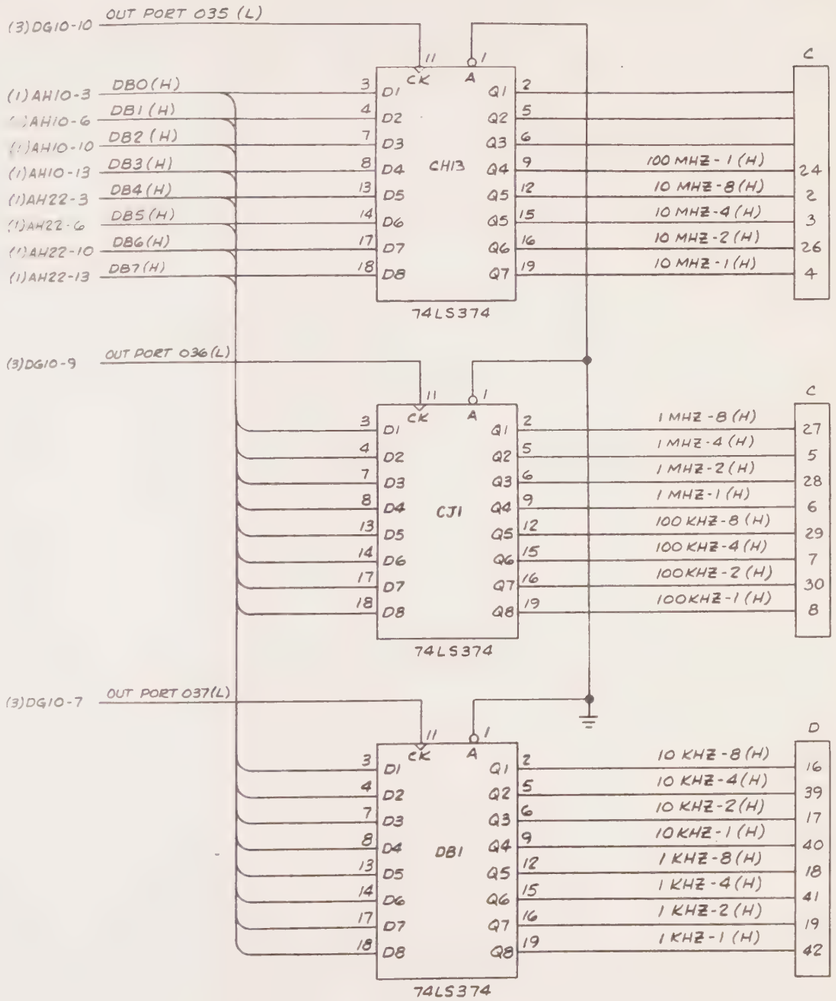
Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 8)

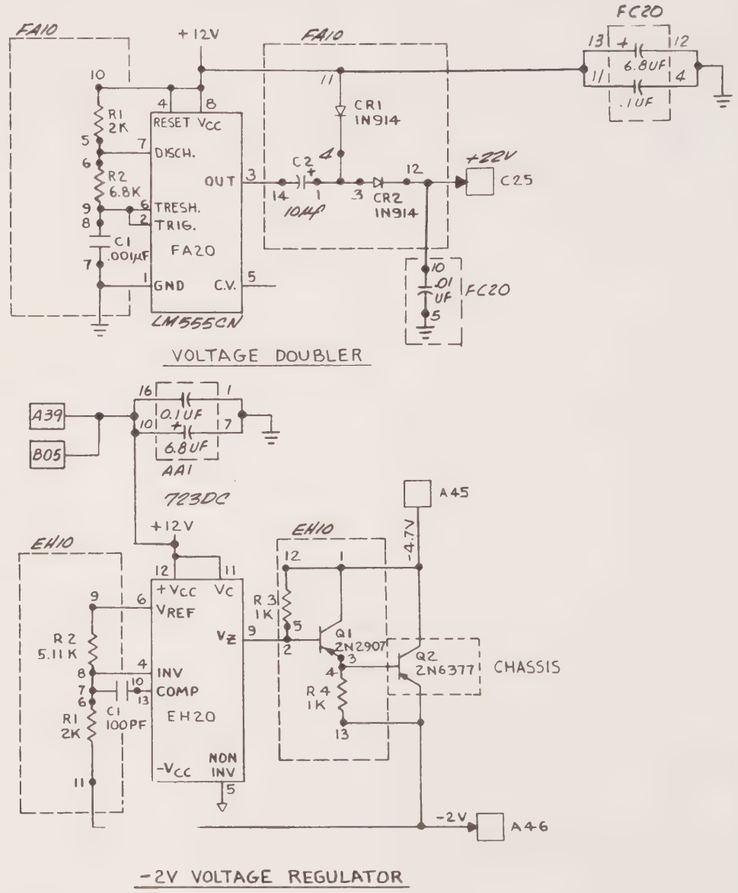


ELECT ALTERABLE ROM

800-0684-2

Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 9)





FREQUENCY SYNTHESIZER OUTPUT BUFFERS

800-0884-2

Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 10)

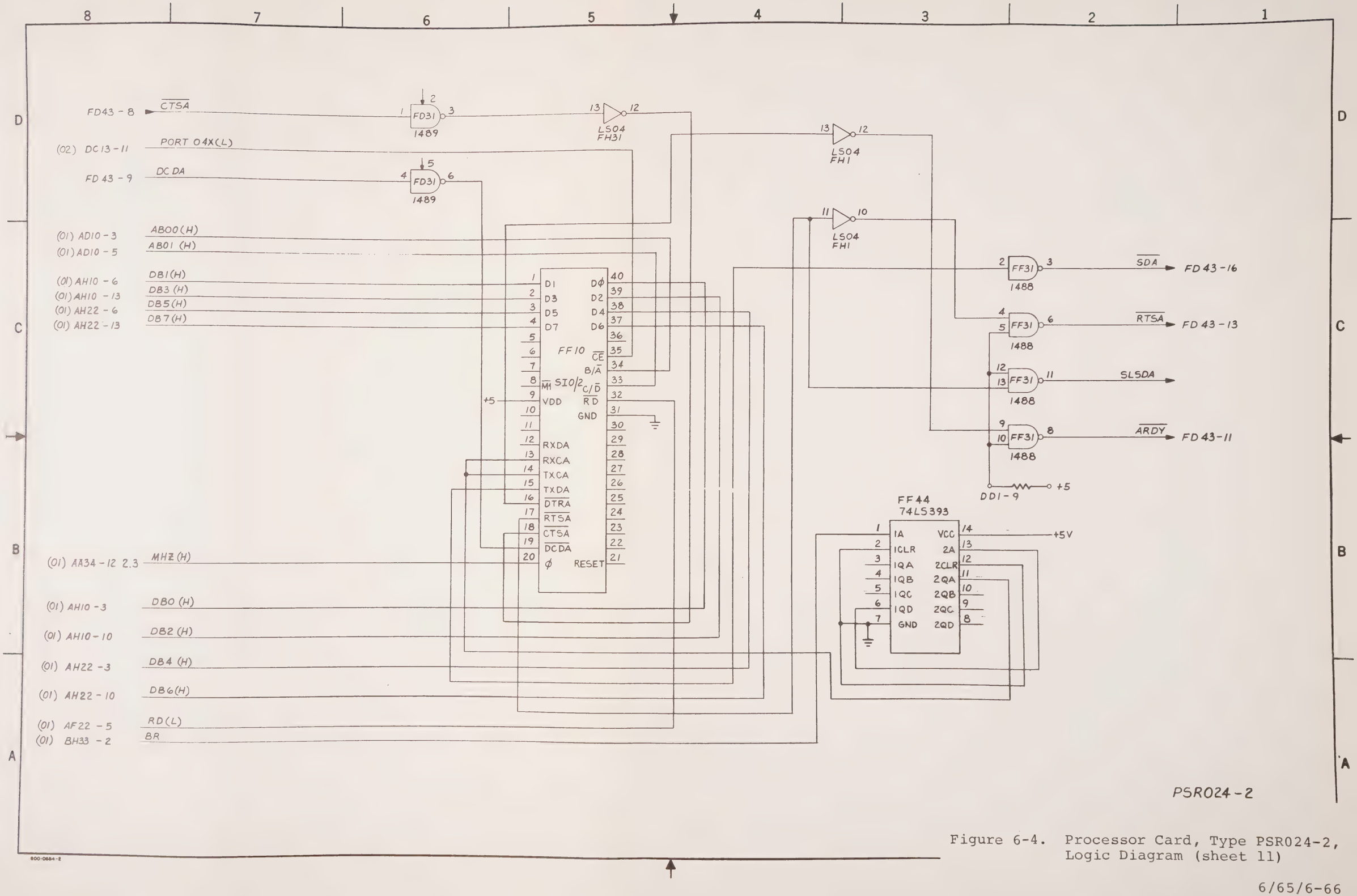


Figure 6-4. Processor Card, Type PSR024-2, Logic Diagram (sheet 11)

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO #06963 JSG	11-17-81	

NOTES:
1. ITEMS #36 & #102 AT LOCATION 5E ARE TO BE INSTALLED ONLY AFTER BOARD MODIFICATION PROCEDURE HAS BEEN COMPLETED.

FOR PARTS LIST SEE PL460-1660-501

Figure 6-5. Transmitter Card, Type GP029-1, Assembly Drawing

Table 6-5

Parts List, GPO29-1 Circuit Card Assy.

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		CIRCUIT CARD ASSY., GPO29-1	20747	460-1660-501	REF
All Capacitors	6-5	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 100 Vdcw	71590	CY30A104M	121
1A		Integrated Circuit AND/OR/INVERT Gate	01295	SN74LS51N-10	1
1B, 1C		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	6
1D, 1E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	8
1FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	5
1G		Integrated Circuit Differential Line Driver/Receiver	07263	F100114DC	6
1GH		Resistor Array, SIP 5-470 ohms, ±2%, 0.9 WATT	71450	750-61-R470	25
1H		Not Used			
1J		Integrated Circuit 4 Stage Counter	07263	F100136DC	7
1JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	39
1K	6-5	Integrated Circuit D-Type Flip-Flop	07263	F100131DC	5

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
1KL	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1L		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	3
1LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1M		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	REF
1MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1NP		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
2A		Resistor Array, Terminating DIP 220/330 ohms, ±5%, 1/4 WATT	73138	898-5-R220/330	2
2B, 2C		Integrated Circuit Line Driver/Receiver	01295	SN74LS241N-10	4
2D		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	8
2E		Oscillator, DIP Crystal 5.6 MHZ	04713	K1144A5.6 MHZ	1
2EF	6-5	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF

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Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
2FF	6-5	Integrated Circuit ECL to TTL Translator	07263	F10125PC	3
2G		Integrated Circuit Differential Line Driver/Receiver	07263	F100114DC	REF
2GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
2H		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	6
2J		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
2JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2K		Integrated Circuit Exclusive OR/NOR Gate	07263	F100107DC	1
2KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2L		Integrated Circuit 9 Bit Comparator	07263	F100166DC	3
2LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2M	6-5	Integrated Circuit 9 Bit Comparator	07263	F100166DC	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
2MN	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2N		Integrated Circuit 9 Bit Comparator	07263	F100166DC	REF
2NP		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
3A		Resistor Array, Terminating DIP 220/330 Ohms, ±2%, 0.9 WATT	73138	898-5-R220/330	REF
3B - 3D		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	7
3E		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
3F		Not Used			
3FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF
3G		Integrated Circuit Differential Line Receiver	07263	F100114DC	REF
3GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
3H		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
3J	6-5	Integrated Circuit 5 Input AND/NOR Gate	07263	F100101DC	2

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
3JK	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
3K		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
3KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
3L - 3N		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	11
4A - 4C		Integrated Circuit 2 to 4 Line Decoder/Multiplexer	01295	SN74LS139N-10	3
4D		Integrated Circuit 8 Bit Parallel Out Serial Shift Register	01295	SN74LS164N-10	2
4E		Integrated Circuit 50 ohm Line Driver	01295	SN74128N-10	2
4EF		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
4FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF
4FG	6-5	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
4G	6-5	Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
4GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
4H		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
4HJ		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4J		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
4JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4K		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
4KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4L - 4N		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
5A, 5B		Integrated Circuit 3 to 8 Line Decoder/Multiplexer	01295	SN74LS138N-10	2
5C	6-5	Integrated Circuit D-Type Flip-Flops	01295	SN74LS374N-10	REF

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Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
5D, 5E	6-5	Integrated Circuit Line Driver/Receiver	01295	SN74LS241N-10	REF
5FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF
5GG		Connector, Coax Adapter	91506	101-HG1	4
5GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
5J		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
5JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
5K - 5M		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
5NP		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6A - 6E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	10
6FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF
6FG		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6G	6-5	Integrated Circuit Differential Line Receiver	07263	F100114DC	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
6GH	6-5	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
6H		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
6HJ		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6J		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6K		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6L		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6M		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6N	6-5	Integrated Circuit 4 Stage Counter	07263	F100136DC	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
6NP	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6X		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	REF
7A - 7C		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
7D		Integrated Circuit Inverter	01295	SN74LS04N-10	2
7E		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
7FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
7G		Integrated Circuit Differential Line Receiver	07263	F100114DC	REF
7GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
7HH		Connector, Coax Adapter	91506	101-HG1	REF
7J		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	REF
7K		Integrated Circuit Differential Line Receiver	07263	F100114DC	REF
7L	6-5	Integrated Circuit 2 Wide OR/AND/OAI Gate	07263	F100117DC	1

Table 6-5
Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
7M	6-5	Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
7N		Integrated Circuit 5 Input OR/NOR Gate	07263	F100101DC	REF
7X		Integrated Circuit 1 of 8 Data Selectors	01295	SN74LS151N-10	2
8A		Integrated Circuit 2 Input Positive NOR Gate	01295	SN74LS02N-10	1
8B		Not Used			
8C		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
8D		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
8E		Integrated Circuit 1 of 8 Data Selector	01295	SN74LS151N-10	REF
8K		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/4 WATT	81349	RC07GF510J	1
8LL,8MM		Connector, Coax Adapter	91506	101-HG1	REF
8MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
8X	6-5	Integrated Circuit 8 Bit Parallel Out Serial Shift Register	01295	SN74LS164N-10	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
9A	6-5	Not Used			
9B - 9E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	REF
9FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
9JK - 9LM 9NP		Resistor Array, SIP 51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
9L		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
9M		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
10A - 10C		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
10D		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
10E		Integrated Circuit 50 ohm Line Driver	01295	SN74128N-10	REF
10FG-10HJ		Resistor Array, SIP 5-51 ohms, ±2%, 0.9 WATT	71450	750-61-R51	REF
10KL		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
10LM	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
10MN, 10NP	6-5	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
11A - 11E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	REF
11EF - 11GH		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
11JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
11KL		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
11LM - 11NP		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
11X		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	REF
12A		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
12B		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
12C		Integrated Circuit Inverter	01295	SN74LS04N-10	REF
12D		Not Used			
12EF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
12FG, 12GH 12JK, 12KL	6-5	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF

Table 6-5

Parts List, GPO29-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
12LM	6-5	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
12NP		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
13A		Not Used			
13C		Integrated Circuit 4 to 10 Line Decoder	01295	SN74LS42N-10	1
13D		Integrated Circuit Line Driver W/3 State Outputs	34335	AM26LS31PC	1
13E		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
15EF,15LF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
JA, JB		Connector, 50 Pin Receptacle	75037	3433-1303	2
JC - JE	6-5	Connector, Coax PC Mount	98291	50-053-0000	3
		Multiwire Board	20747	402-0001-001	1

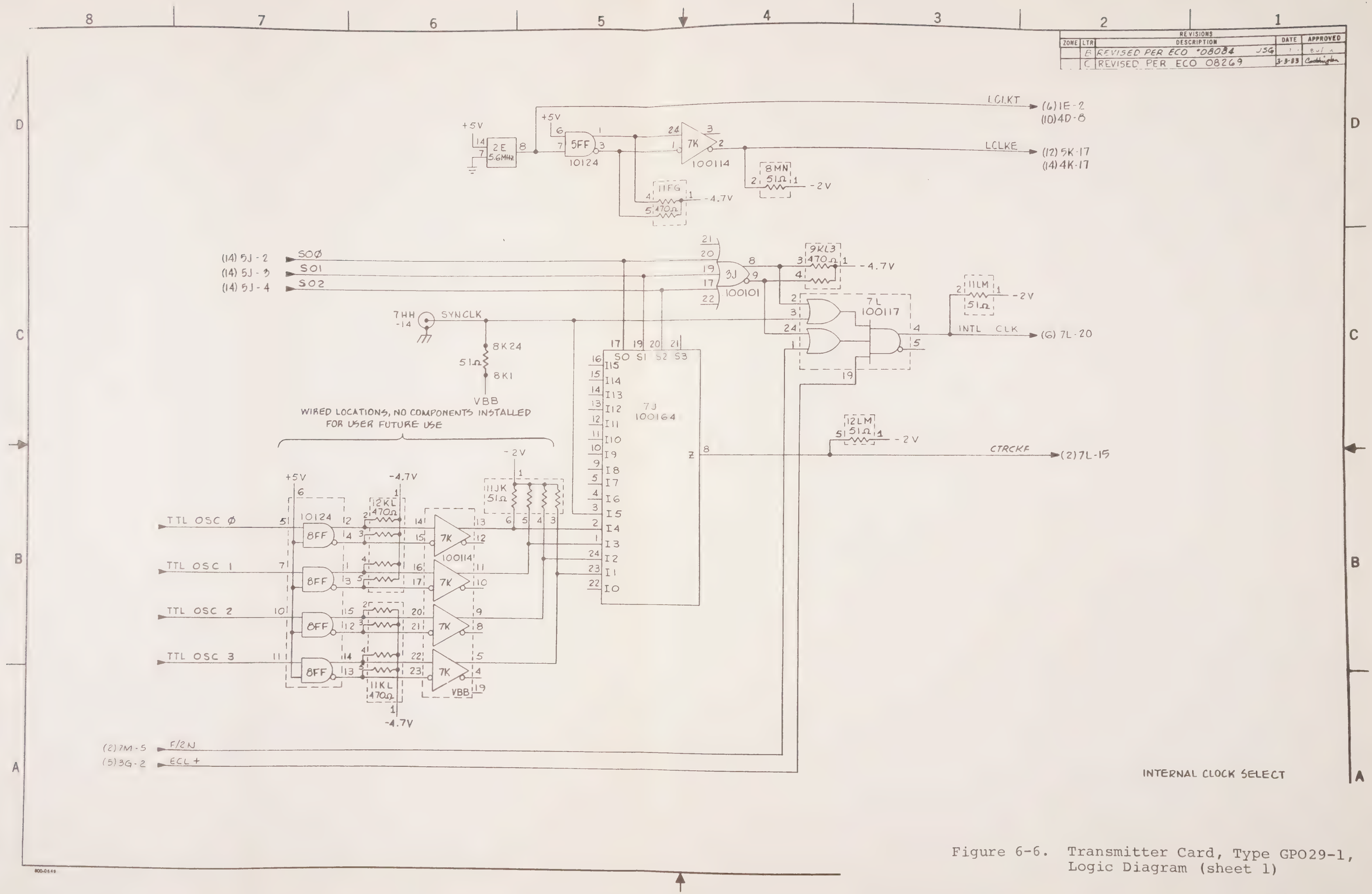


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 1)

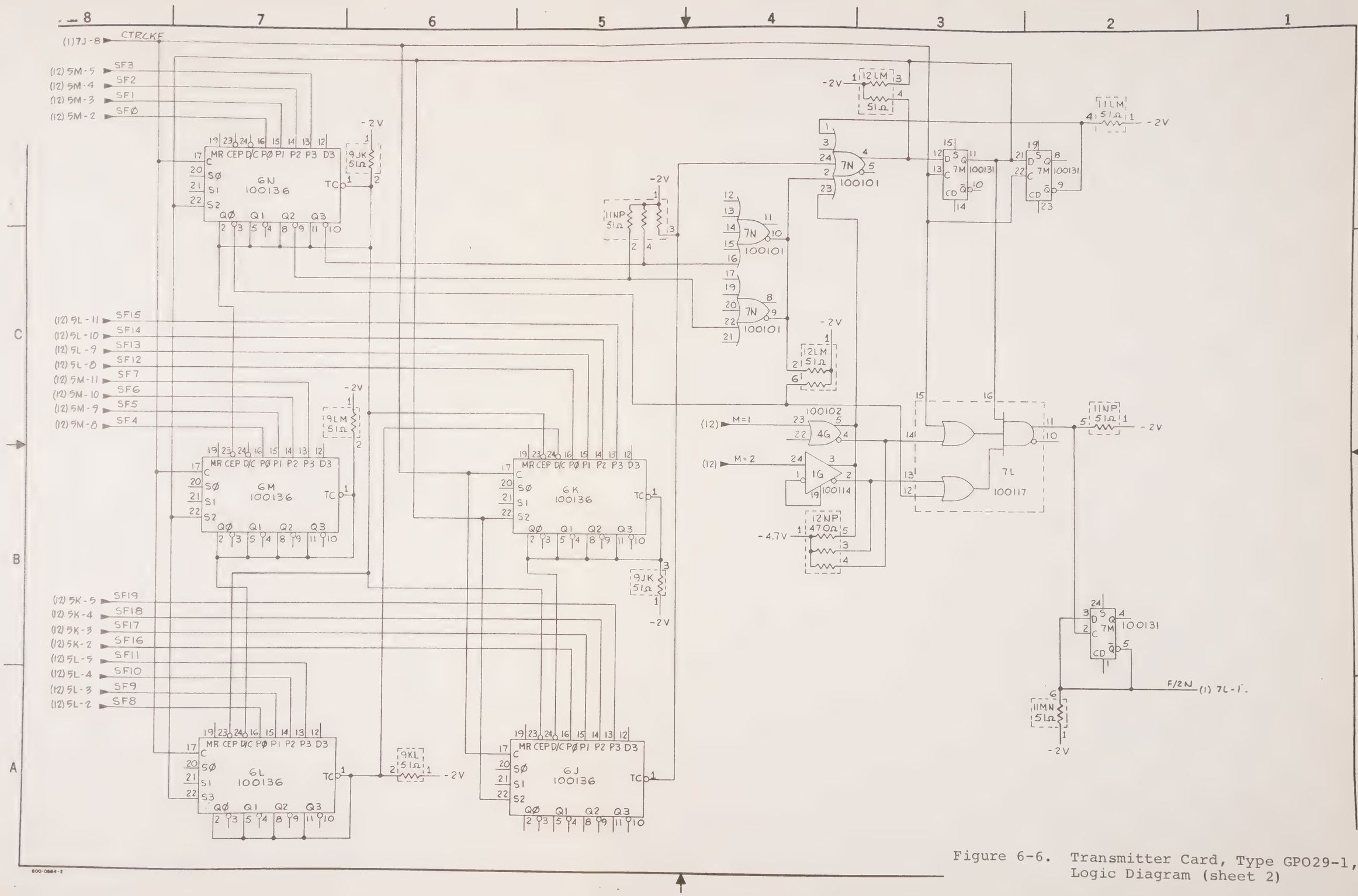


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 2)

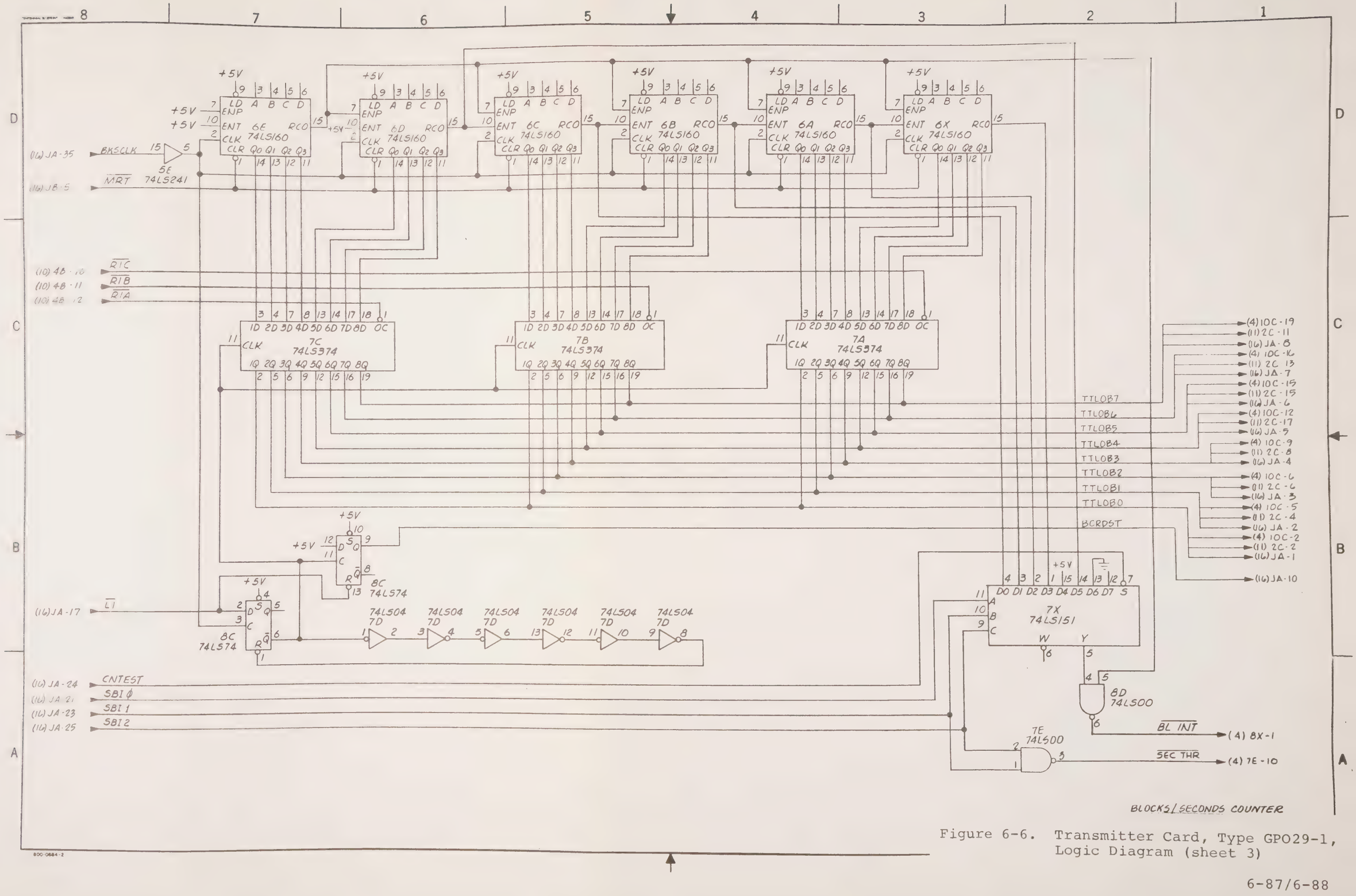


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 3)

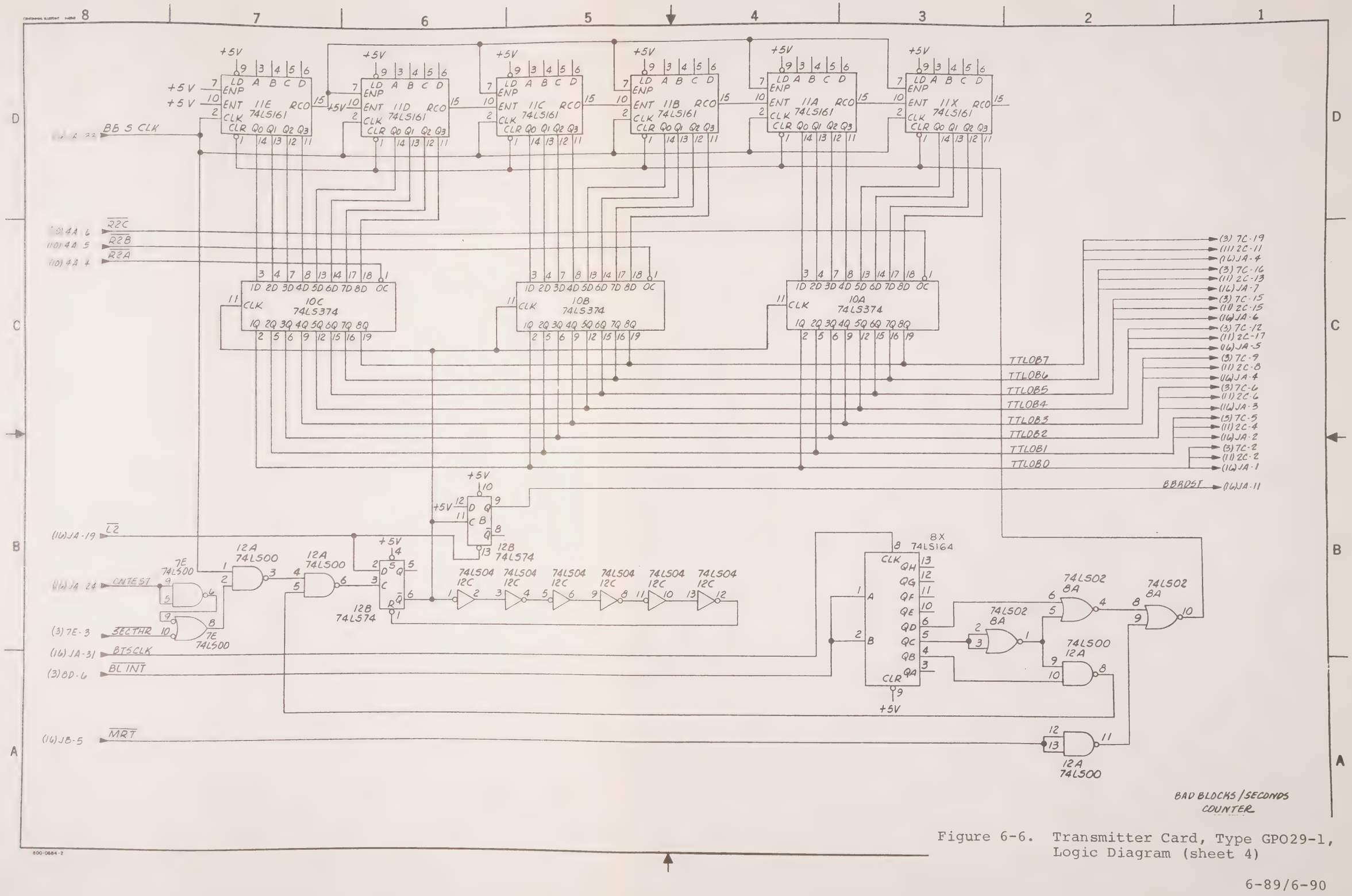


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 4)

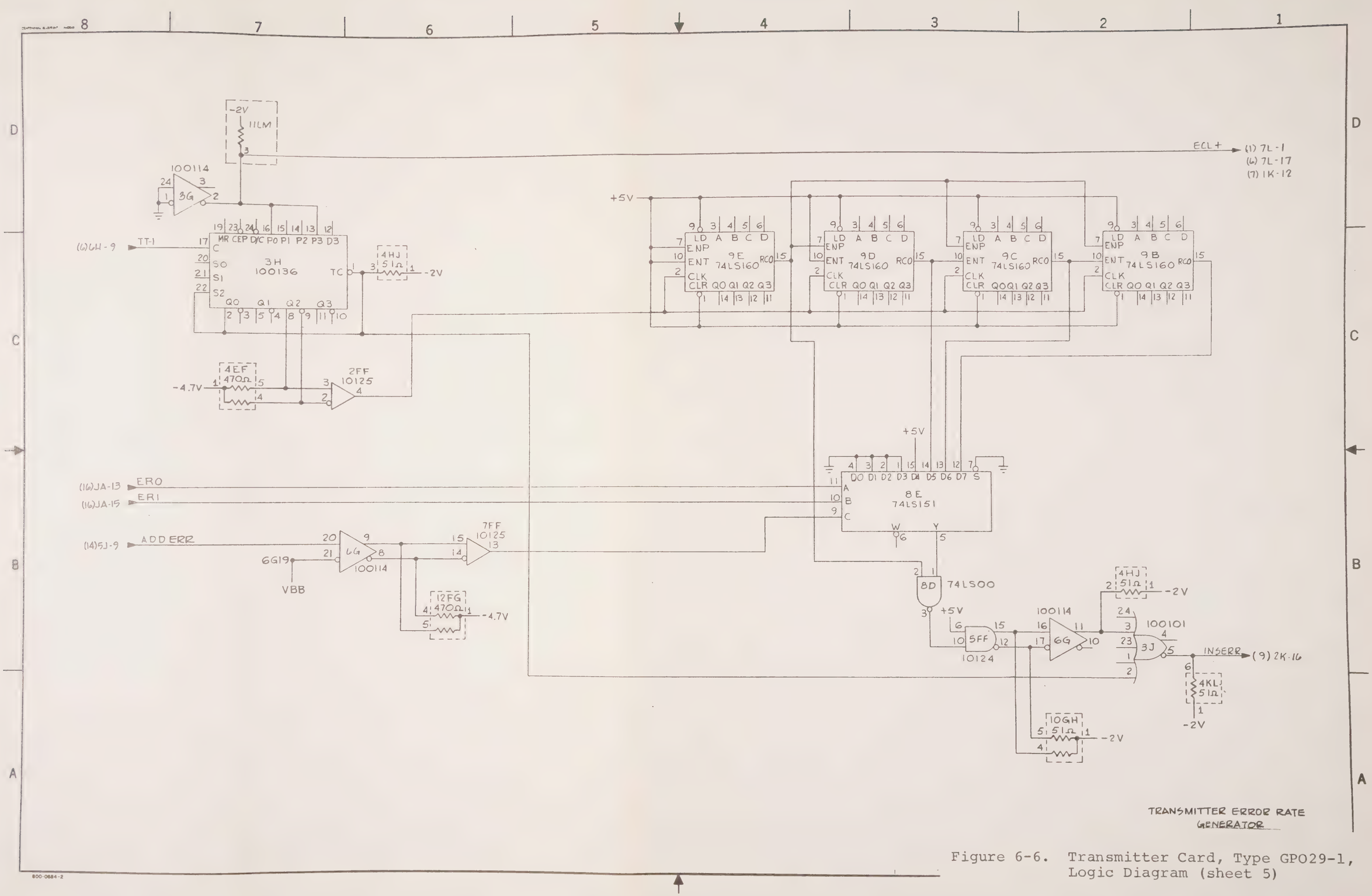


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 5)

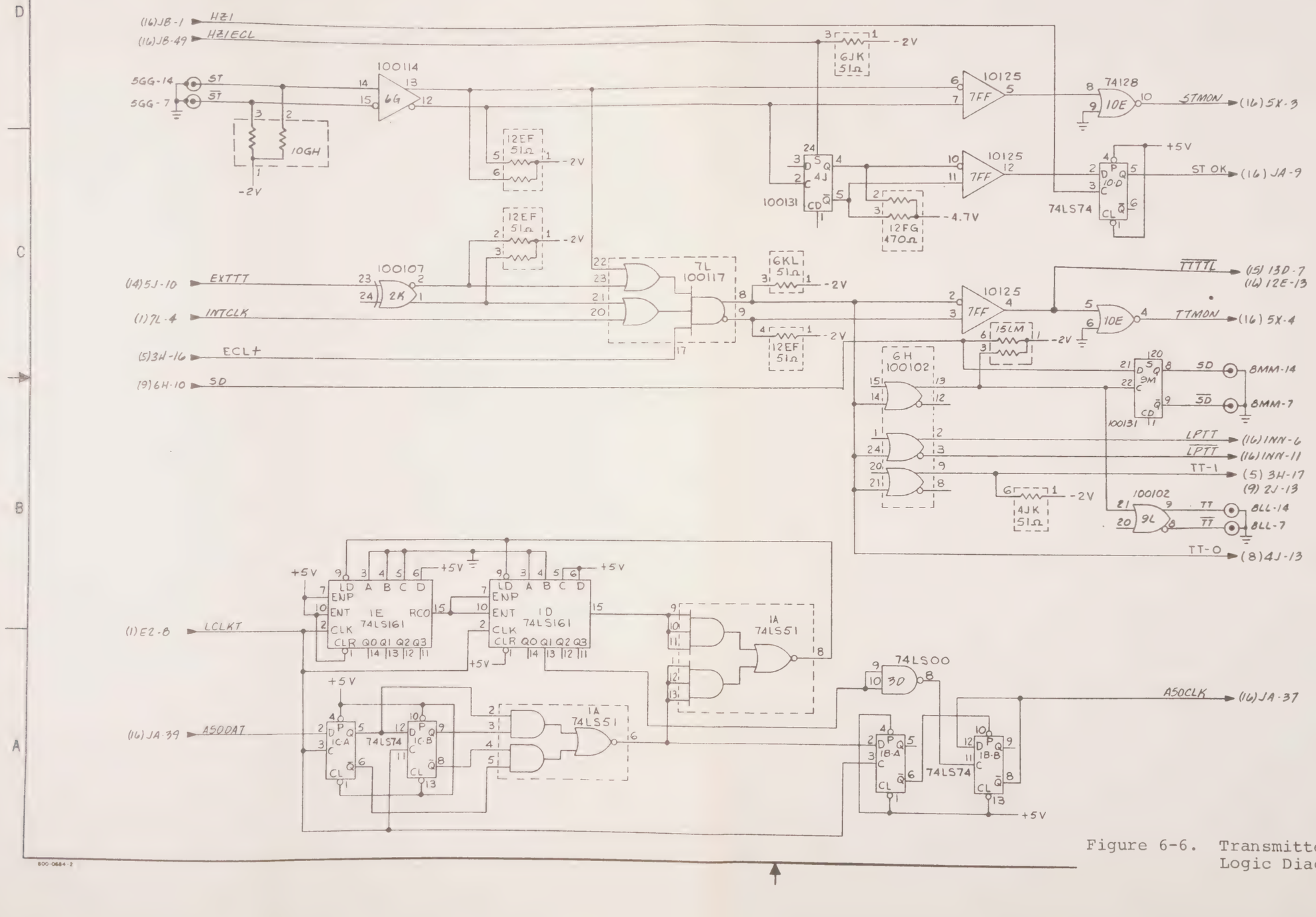


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 6)

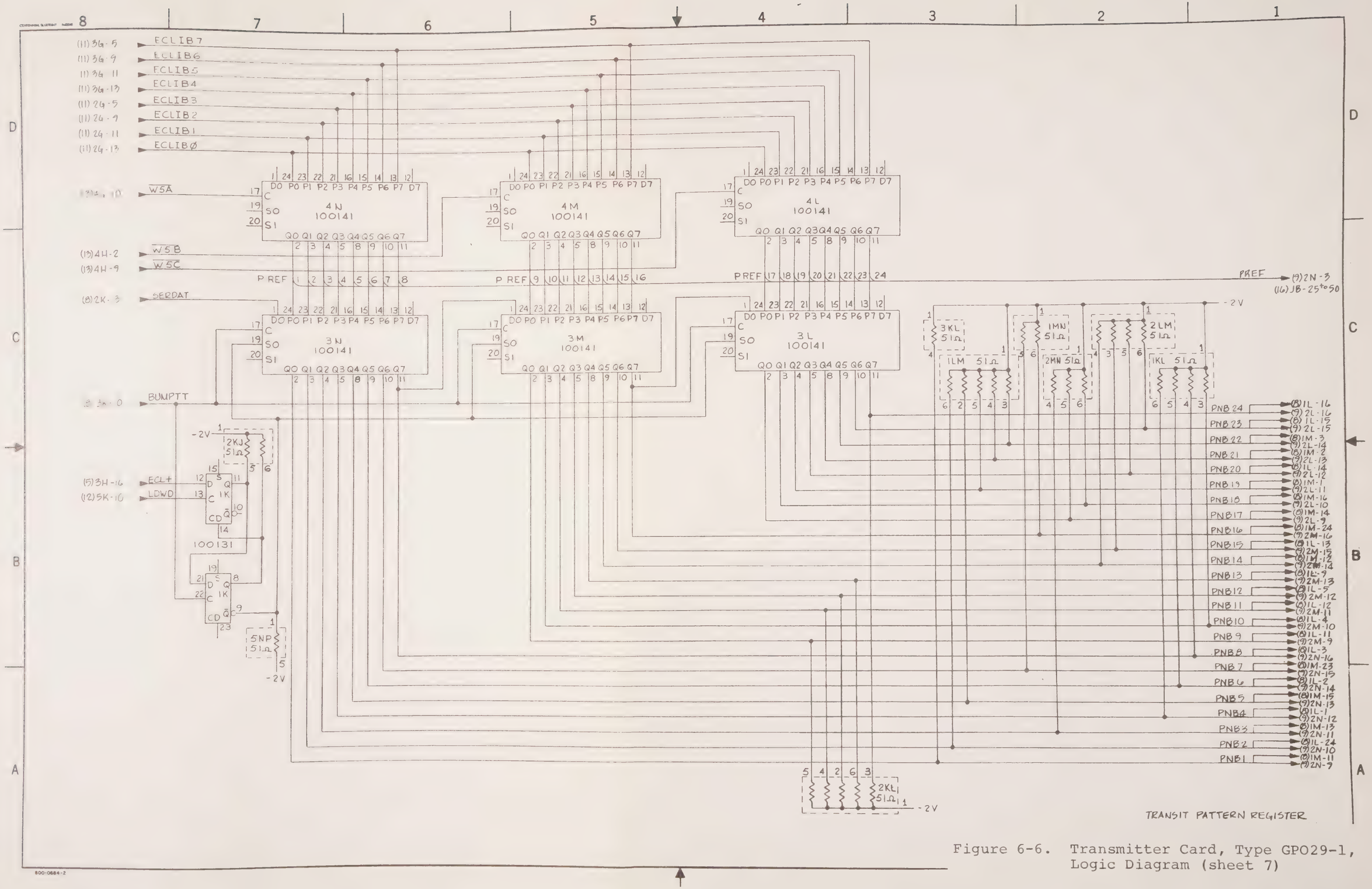


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 7)

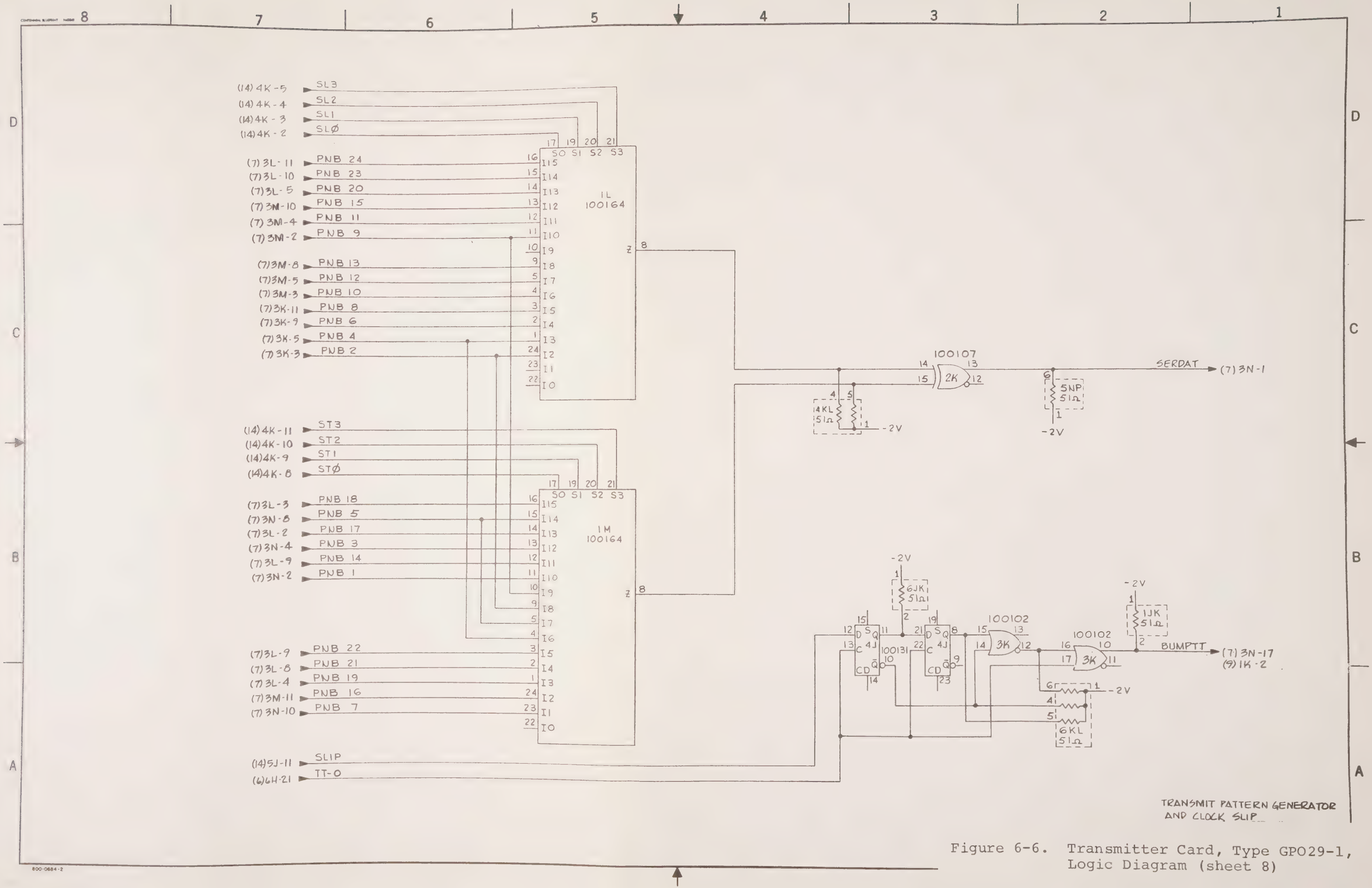


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 8)

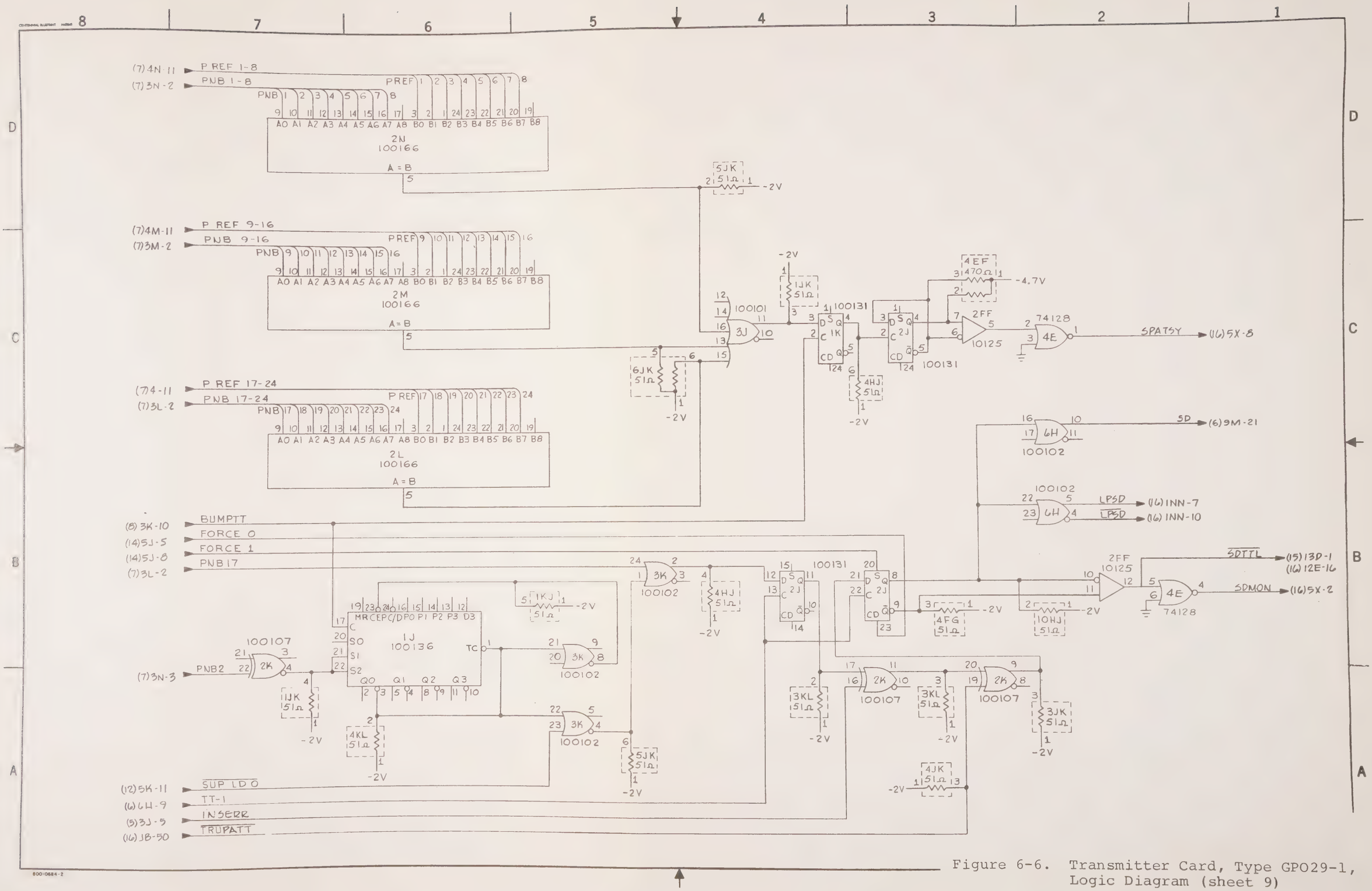


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 9)

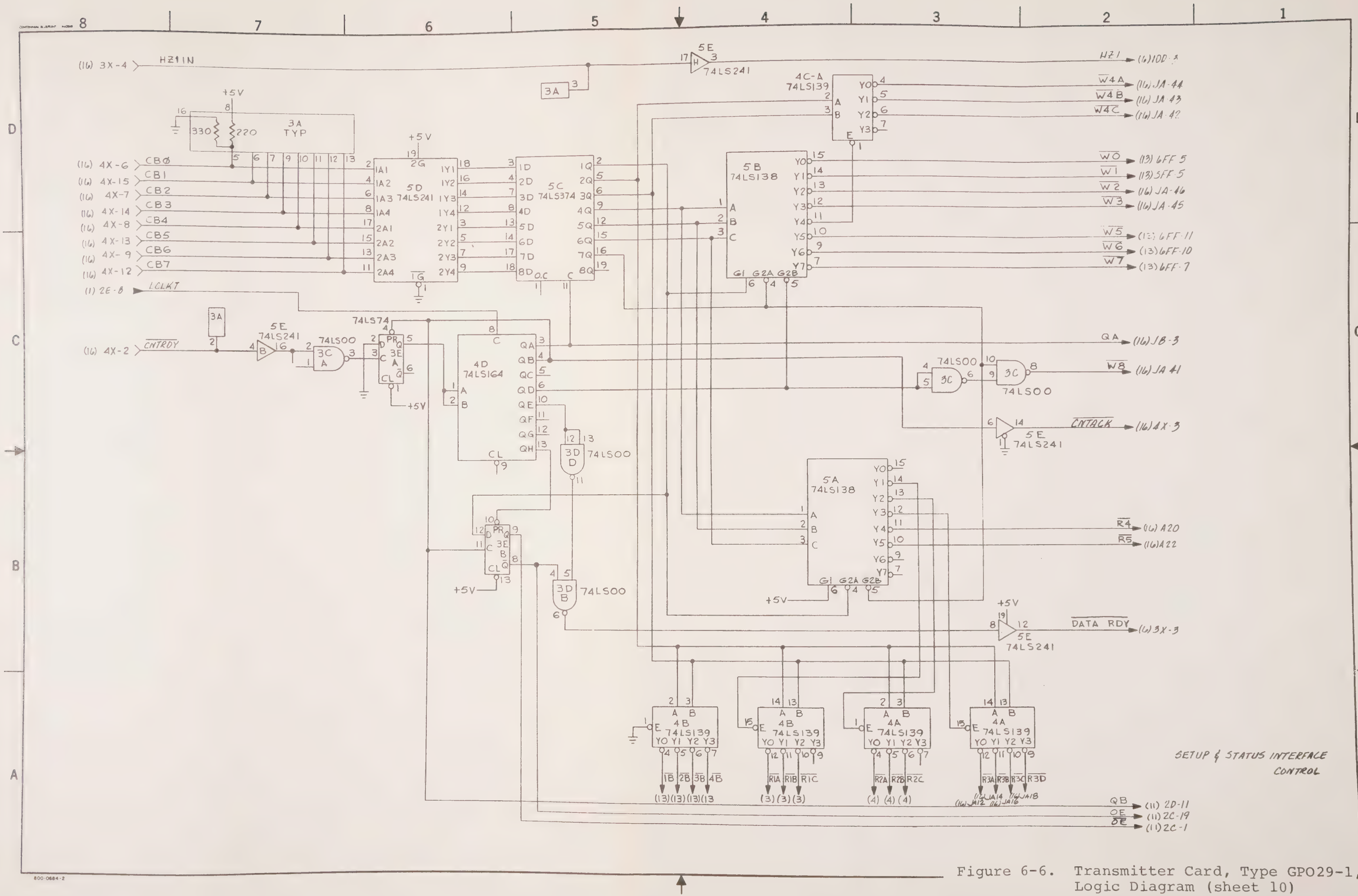


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 10)

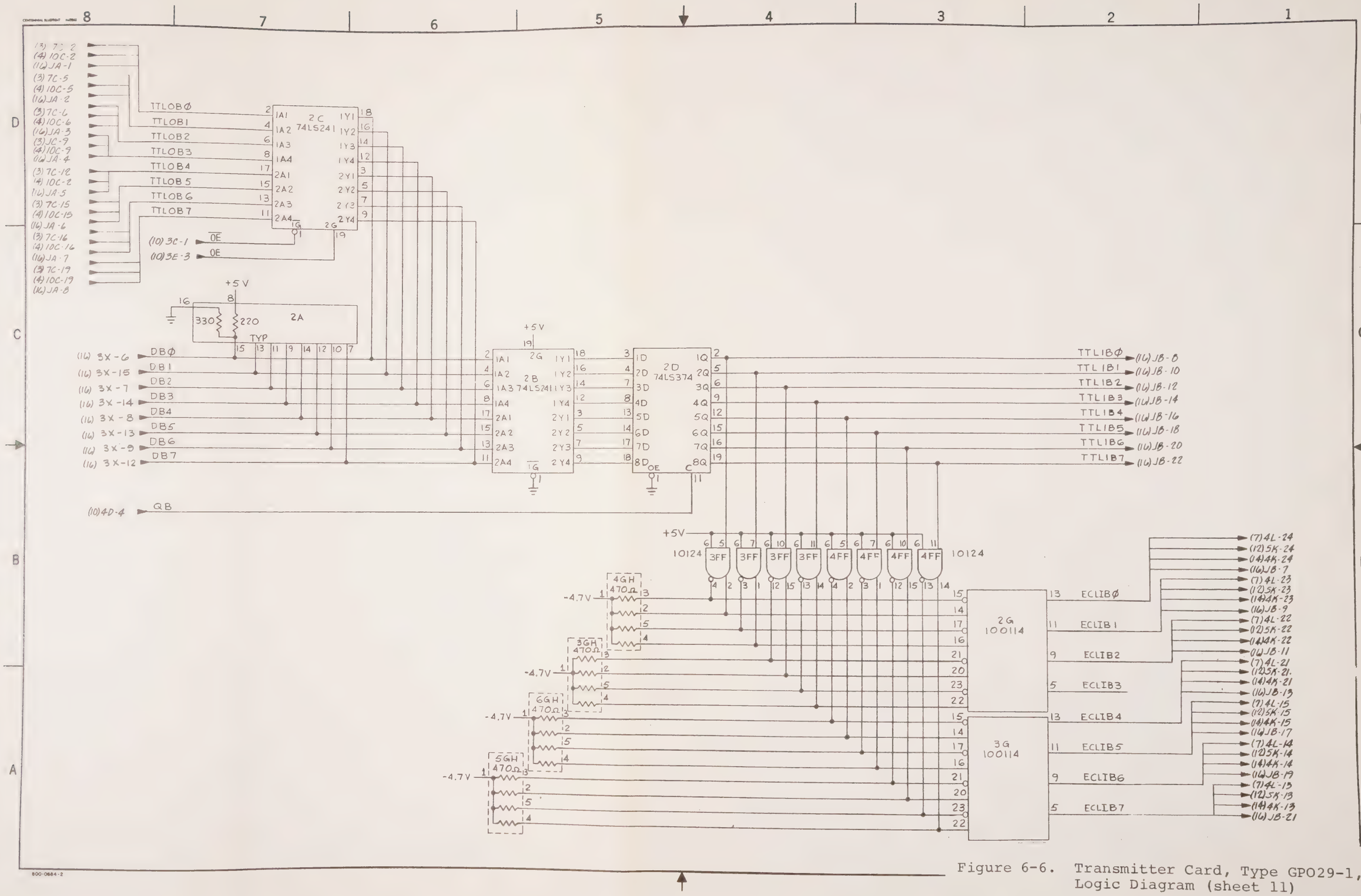


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 11)

(11) 3G - 5 ECLIB7
(11) 3G - 9 ECLIB6
(11) 3G - 11 ECLIB5
(11) 3G - 13 ECLIB4
(11) 2G - 5 ECLIB3
(11) 2G - 9 ECLIB2
(11) 2G - 11 ECLIB1
(11) 2G - 13 ECLIB0
(1) 7K - 2 LCLKE
(13) 4H - 10 $\overline{\text{W1C}}$
(13) 4H - 5 $\overline{\text{W1B}}$
(13) 4G - 13 $\overline{\text{W1A}}$

5M 100141

5L 100141

5K 100141

10LM 51Ω

10KL 470Ω

4FG 470Ω

4JK 51Ω

10JK 470Ω

2KL 51Ω

10NP 470Ω

10MN 470Ω

-4.7V

-2V

$\overline{\text{SUPLD0}}$ (9) 3K-23
LDWD (7) 1K-13
M=2 (2) 1G-24
M=1 (2) 4G-23
SF19 (2) 6J-13
SF18 (2) 6J-14
SF17 (2) 6J-15
SF16 (2) 6J-16
SF15 (2) 6K-13
SF14 (2) 6K-14
SF13 (2) 6K-15
SF12 (2) 6K-16
SF11 (2) 6L-13
SF10 (2) 6L-14
SF9 (2) 6L-15
SF8 (2) 6L-16
SF7 (2) 6M-13
SF6 (2) 6M-14
SF5 (2) 6M-15
SF4 (2) 6M-16
SF3 (2) 6N-13
SF2 (2) 6N-14
SF1 (2) 6N-15
SF0 (2) 6N-16

SETUP REGISTER 1A, 1B, 1C

800-0684-2

Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 12)

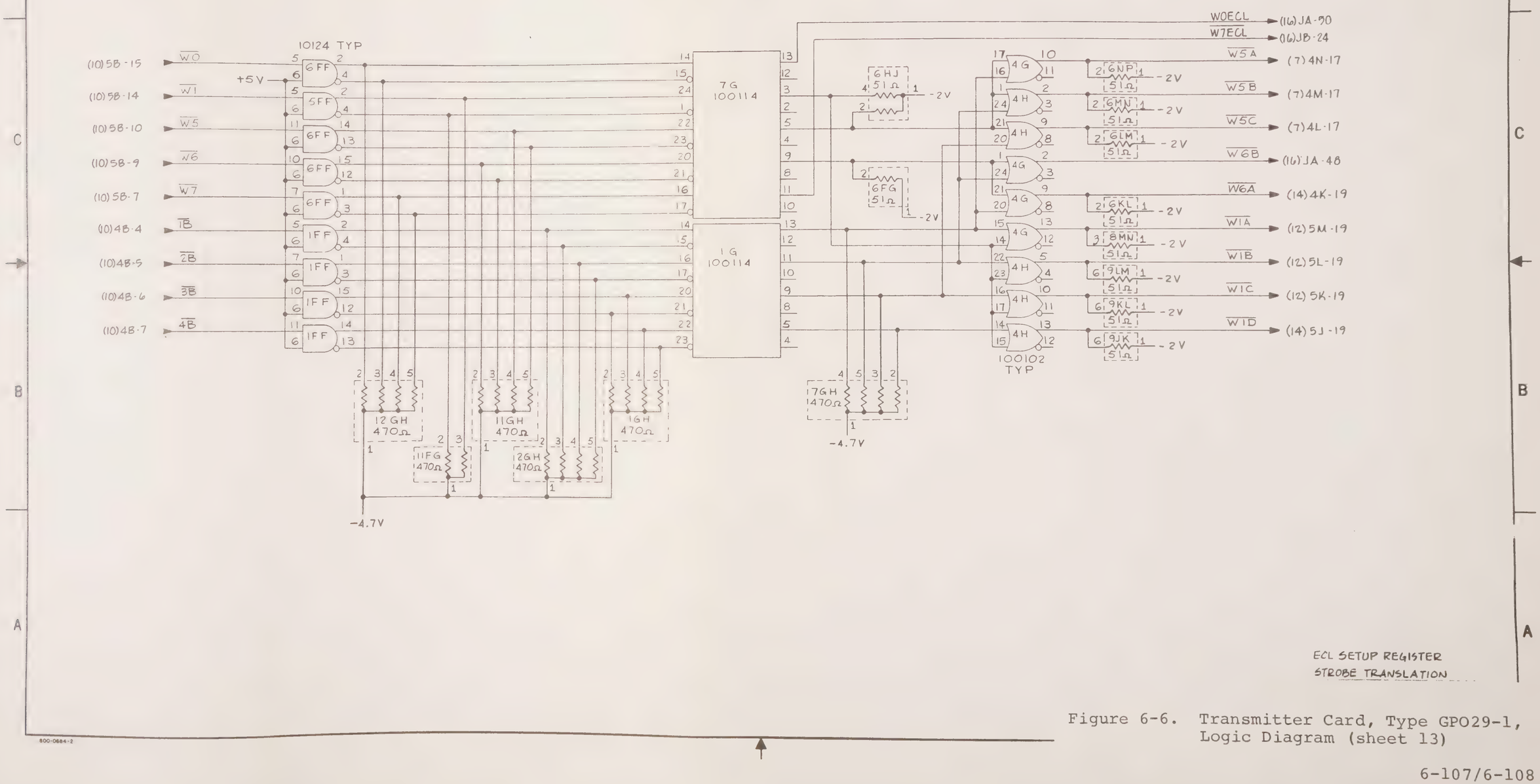


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 13)

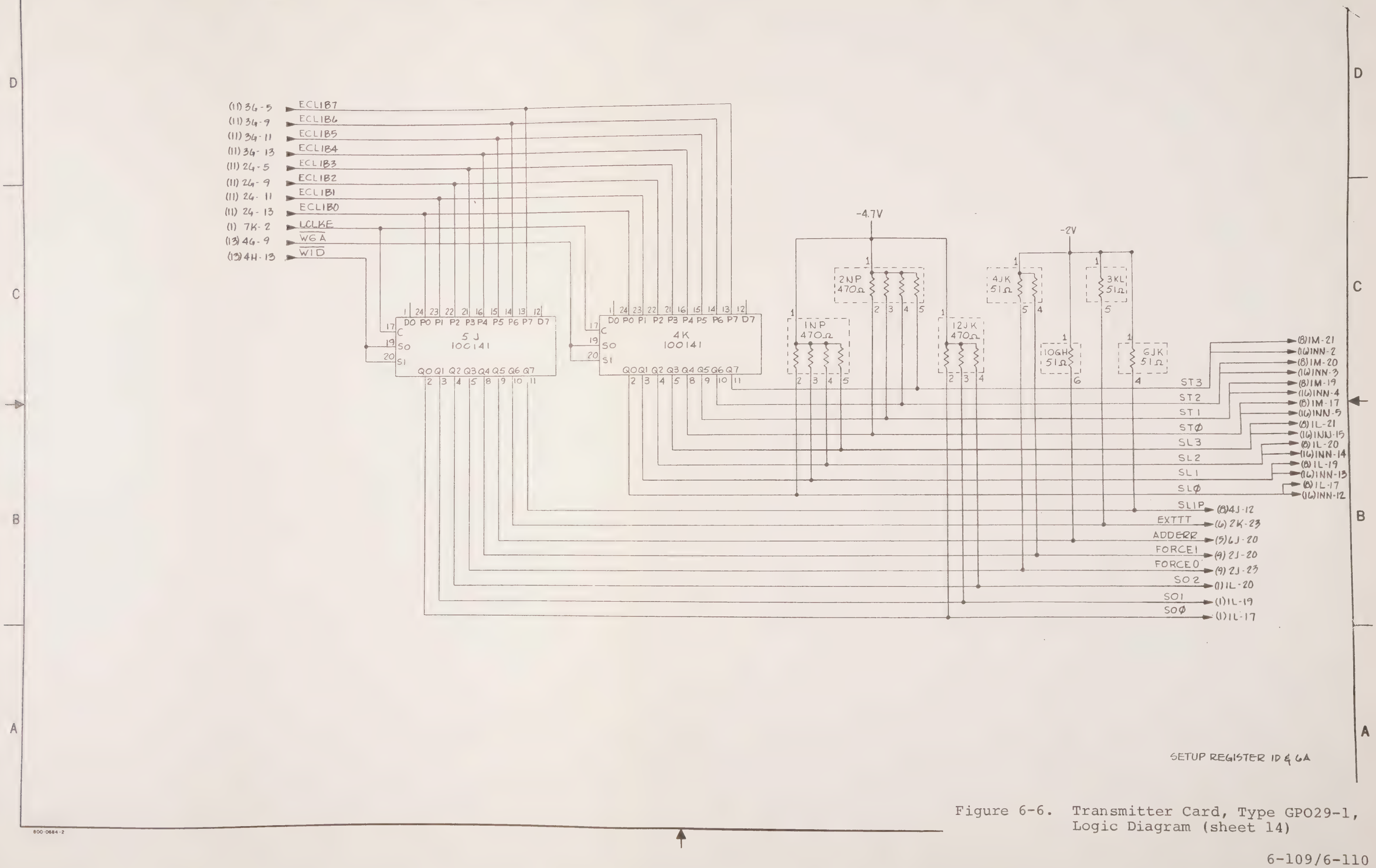


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 14)

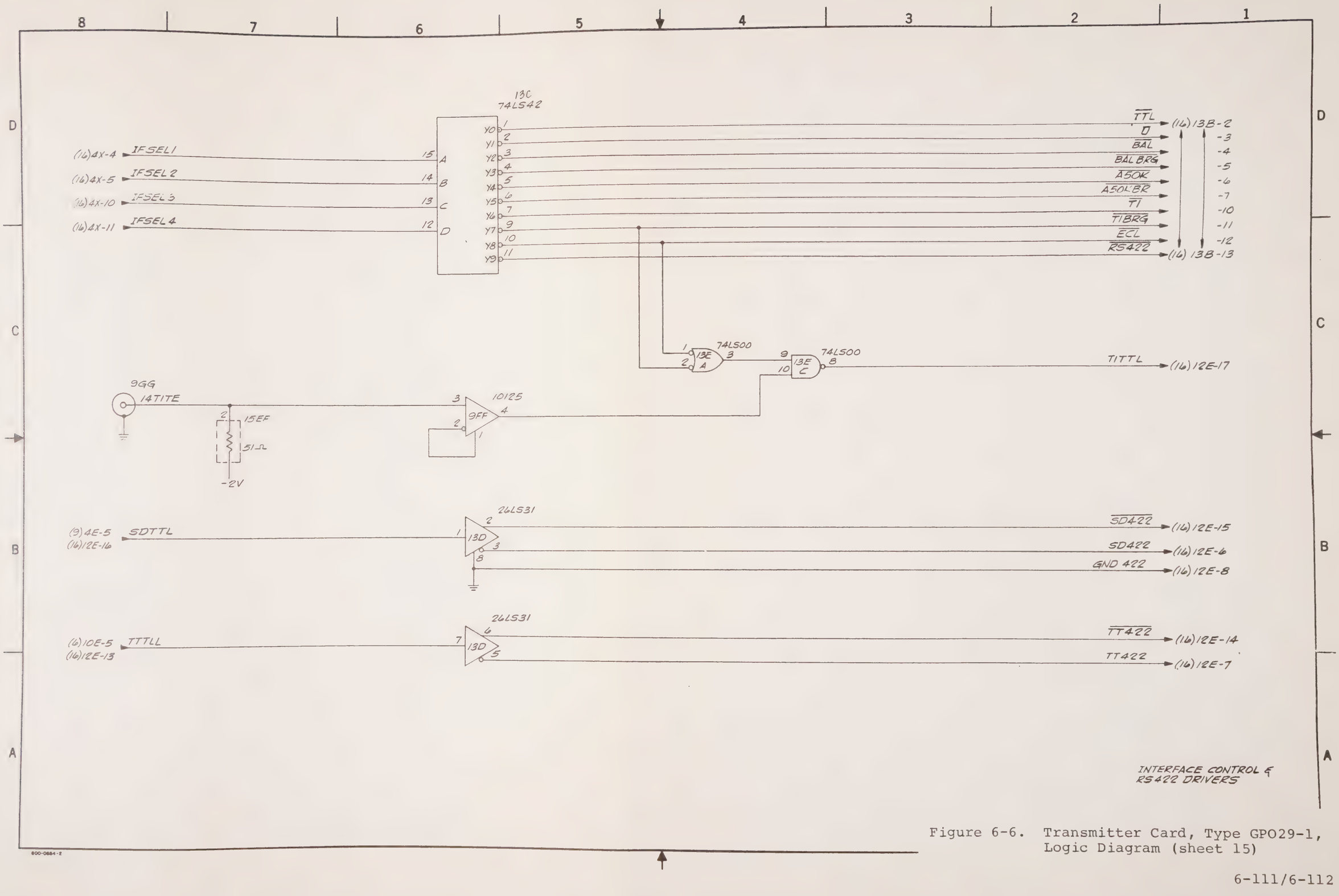


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 15)

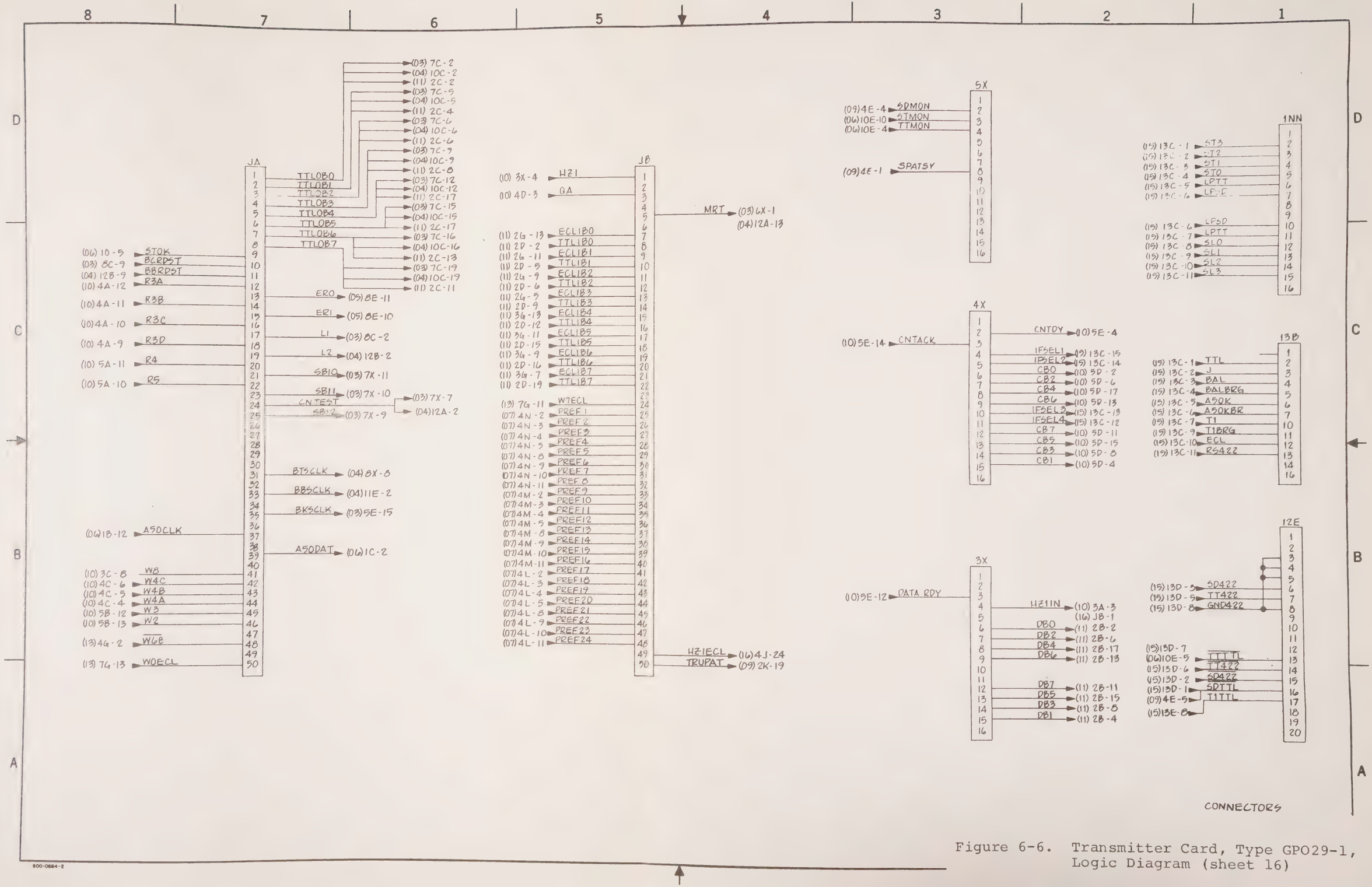
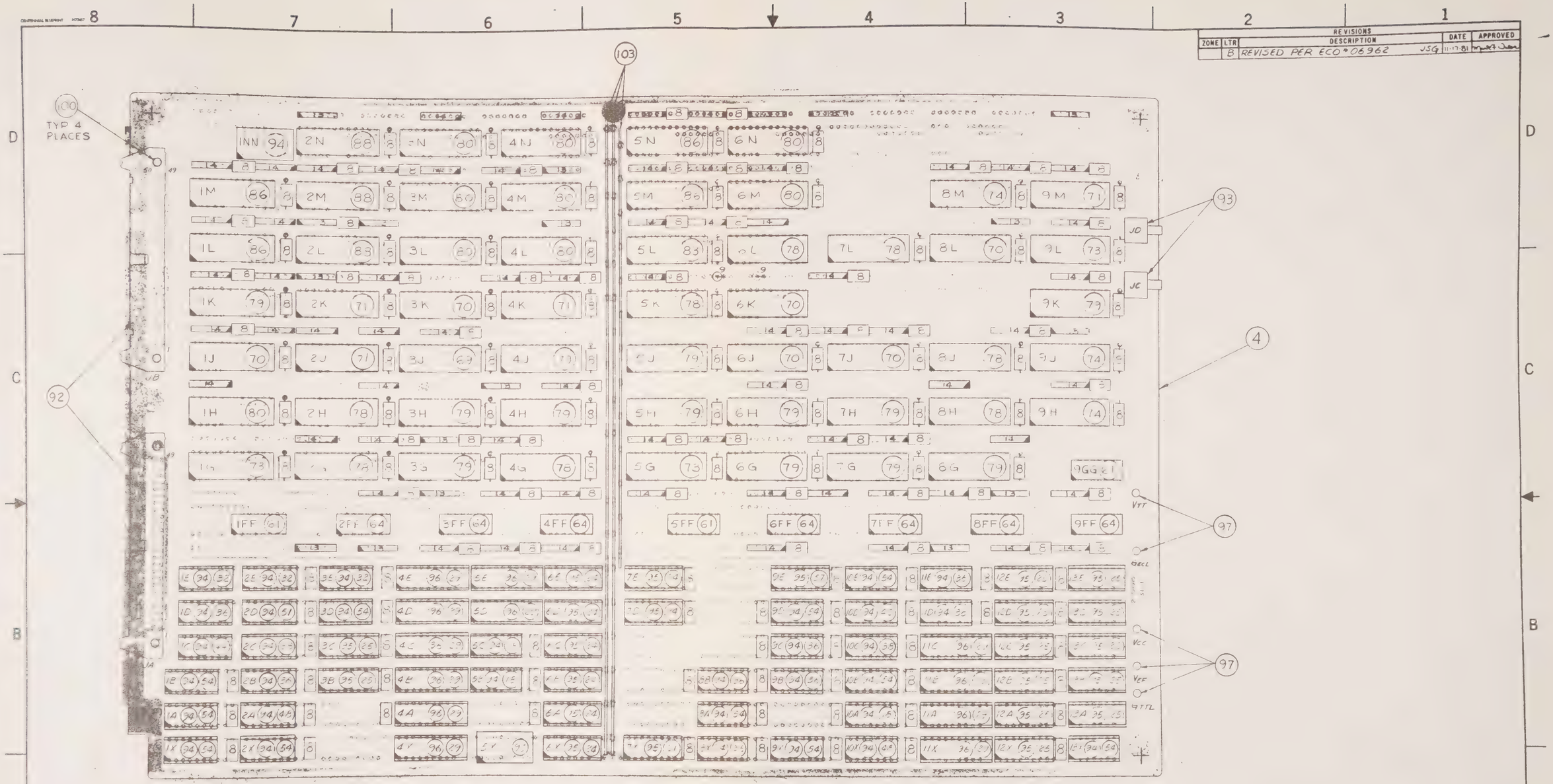


Figure 6-6. Transmitter Card, Type GPO29-1, Logic Diagram (sheet 16)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO #06962	11-17-81	



FOR PARTS LIST SEE PL460-1713-501

Figure 6-7. Receiver Card, Type GP031-1, Assembly Drawing

Table 6-6

Parts List, GP031-1 Circuit Card Assy.

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		CIRCUIT CARD ASSY., GP031-1	20747	460-1713-501	REF
All Capacitors	6-7	Capacitor, Fxd. Ceramic 0.1 uf, ±2%, 100 Vdcw	71590	CY30A104M	155
1A, 1B		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	11
1C		Integrated Circuit 4 Input Positive NAND Gate	01295	SN74LS20N-10	1
1D		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	7
1E		Integrated Circuit 4 Bit Binary Counter	01295	SN74LS393N-10	3
1FF		Integrated Circuit TTL to ECL Translator	07263	F10124PC	3
1G		Integrated Circuit Differential Line Receiver	07263	F100114DC	3
1H		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	9
1HJ		Resistor Array SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	69
1J		Integrated Circuit 2 Input or NOR Gate	07263	F100102DC	6
1JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1K	6-7	Integrated Circuit 4 Stage Counter	07263	F100136 DC	13

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
1KL	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1L		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	4
1LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1M		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	REF
1MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
1X		Integrated Circuit D-Type Flip-Flops	01295	SN74LS74N-10	REF
2A		Integrated Circuit 8 Input Positive NAND Gate	01295	SN74LS30N-10	2
2B		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
2C		Integrated Circuit 2 Input Positive NOR Gate	01295	SN74LS02N-10	3
2D		Integrated Circuit AND/OR/INVERT Gate	01295	SN74LS51N-10	1
2E	6-7	Integrated Circuit 4 Bit Binary Counter	01295	SN74LS393N-10	REF

800-0566A

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
2FF	6-7	Integrated Circuit ECL to TTL Translator	07263	F10125PC	7
2G, 2H		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	8
2J		Integrated Circuit Exclusive OR/NOR Gate	07263	F100107DC	4
2JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2K		Integrated Circuit Exclusive OR/NOR Gate	07263	F100107DC	REF
2KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2L		Integrated Circuit 9 Bit Comparator	07263	F100166DC	3
2LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2M		Integrated Circuit 9 Bit Comparator	07263	F100166DC	REF
2MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
2N		Integrated Circuit 9 Bit Comparator	07263	F100166DC	REF
2X	6-7	Integrated Circuit D-Type Flip-Flops	01295	SN74LS74N-10	REF
3A		Not Used			

Table 6-6

Parts List, GPO31-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
3B, 3C	6-7	Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	13
3D		Integrated Circuit D-Type Flip-Flops	01295	SN74LS74N-10	REF
3E		Integrated Circuit 4 Bit Binary Counter	01295	SN74LS393N-10	REF
3EF		Resistor Array, SIP 5-470 Ohm, ±2%, 0.9 WATT	71450	750-61-R470	18
3FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
3G, 3H		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
3GH		Resistor Array, SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
3J		Integrated Circuit 5 Input OR/NOR Gate	07263	F100101DC	1
3K		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
3JK		Resistor Array, SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
3KL		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
3L		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
3LM		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
3M	6-7	Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
3MN	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
3N		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
3NP		Resistor Array, SIP 5-470 Ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
4A - 4E		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	12
4EF		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
4FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
4FG		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4G		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
4GH		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4H		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
4HJ		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4J		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
4JK		Resistor Array, SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4K	6-7	Integrated Circuit Exclusive OR/NOR Gate	07263	F100107DC	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
4KL	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4L		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
4LM		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
4M		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
4MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
4N		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
4X		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
5A		Not Used			
5B, 5C		Integrated Circuit 50 ohm Line Driver	01295	SN74128N-10	3
5D, 5E		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
5EF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
5FF	6-7	Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
5FG	6-7	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
5G		Integrated Circuit Differential Line Receiver	07263	F100114DC	REF
5GH		Resistor Array, SIP 5-470 ohm ±2%, 0.9 WATT	71450	750-61-R470	REF
5H, 5J		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
5JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
5K		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
5KK		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/4 WATT	81349	RC07GF510J	2
5L		Integrated Circuit D-Type Flip-Flop	07263	F100151DC	1
5M, 5N		Integrated Circuit 16 Input Multiplexer	07263	F100164DC	REF
5MN,5NP		Resistor Array, SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6A - 6E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	8
6EF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6FF	6-7	Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
6FG	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6G		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6GH		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6H		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
6HJ		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
6J,6K		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
6KK		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/4 WATT	81349	RC07GF510J	REF
6KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6L		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
6M		Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF
6MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
6N	6-7	Integrated Circuit 8 Bit Universal Shift Register	07263	F100141DC	REF

Table 6-6

Parts List, GPO31-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
6X	6-7	Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	REF
7A - 7C		Not Used			
7D, 7E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS160N-10	REF
7EF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
7FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
7FG		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
7G, 7H		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
7HJ		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
7J		Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REF
7K		Not Used			
7KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
7L	6-7	Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
7LM, 7MN	6-7	Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
7NP		Resistor Array, SIP 5-51 Ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
7X		Integrated Circuit 1 of 8 Data Selectors	01295	SN74LS151N-10	1
8A		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
8B		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
8C - 8E		Not Used			
8FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
8FG		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
8G		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
8GH		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
8H, 8J		Integrated Circuit D-Type Flip-Flop	07263	F100131DC	REF
8KL	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
8L	6-7	Integrated Circuit 2 Input OR/NOR Gate	07263	F100102DC	REV
8LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
8M		Integrated Circuit 2 Wide OR/AND/OAI Gate	07263	F100117DC	3
8MN, 8NP		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
8X		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
9A		Not Used			
9B, 9C		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
9D		Integrated Circuit D-Type FLip-Flop	01295	SN74LS74N-10	REF
9E		Integrated Circuit 4 Bit Magnitude Comparator	01295	SN74LS85N-10	1
9FF		Integrated Circuit ECL to TTL Translator	07263	F10125PC	REF
9GG		Integrated Circuit TTL to ECL Translator	07263	F10124PC	REF
9GH	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
9H, 9J	6-7	Integrated Circuit 2 Wide OR/AND/OAI Gate	07263	F100117DC	REF
9K		Integrated Circuit 4 Stage Counter	07263	F100136DC	REF
9L		Integrated Circuit Differential Line Receiver	07263	F100114DC	REF
9LM		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
9M		Integrated Circuit Exclusive OR/NOR Gate	07263	F100107DC	REF
9MN, 9NP		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
9X		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
10A		Integrated Circuit 50 ohm Line Driver	01295	SN74128N-10	REF
10B		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
10C		Integrated Circuit 2 Input Positive NOR Gate	01295	SN74LS02N-10	REF
10D		Integrated Circuit Inverter	01295	SN74LS04N-10	1
10E	6-7	Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF

Table 6-6

Parts List, GPO31-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
10EF, 10FG, 10HJ, 10JK, 10LM, 10MN	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
10NP		Resistor Array, SIP 5-470 Ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
10X		Integrated Circuit 8 Input Positive NAND Gate	01295	SN74LS30N-10	REF
11A - 11C		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
11D		Integrated Circuit 2 Input Positive NOR Gate	01295	SN74LS02N-10	REF
11E		Integrated Circuit 2 Input NAND Gate	01295	SN74LS00N-10	REF
11FG, 11GH, 11JK, 11KL		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
11NP		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
11X		Integrated Circuit D-Type Flip-Flop	01295	SN74LS374N-10	REF
12A - 12E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	REF
12EF, 12FG, 12GH, 12JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
12X, 13A - 13E		Integrated Circuit Synchronous 4 Bit Counter	01295	SN74LS161N-10	REF
13EF	6-7	Resistor Array, SIP 5-470 Ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF

Table 6-6

Parts List, GP031-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
13FG, 13HJ, 13MN	6-7	Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
13X		Integrated Circuit D-Type Flip-Flop	01295	SN74LS74N-10	REF
14EF		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
14FG		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
14GH,14JK		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
14LM		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
14MN, 15EF, 15FG, 15HJ		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
15JK		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
15KL, 15LM, 15MN		Resistor Array, SIP 5-51 ohm, ±2%, 0.9 WATT	71450	750-61-R51	REF
15NP		Resistor Array, SIP 5-470 ohm, ±2%, 0.9 WATT	71450	750-61-R470	REF
JA, JB		Connector, 50 Pin Receptacle	75037	3433-1303	2
JC - JE	6-7	Connector, Coax PC Mount	98291	50-053-0000	3

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 08084 WKH	12-15-82	
	C	REVISED PER ECO 08269	3-3-83	

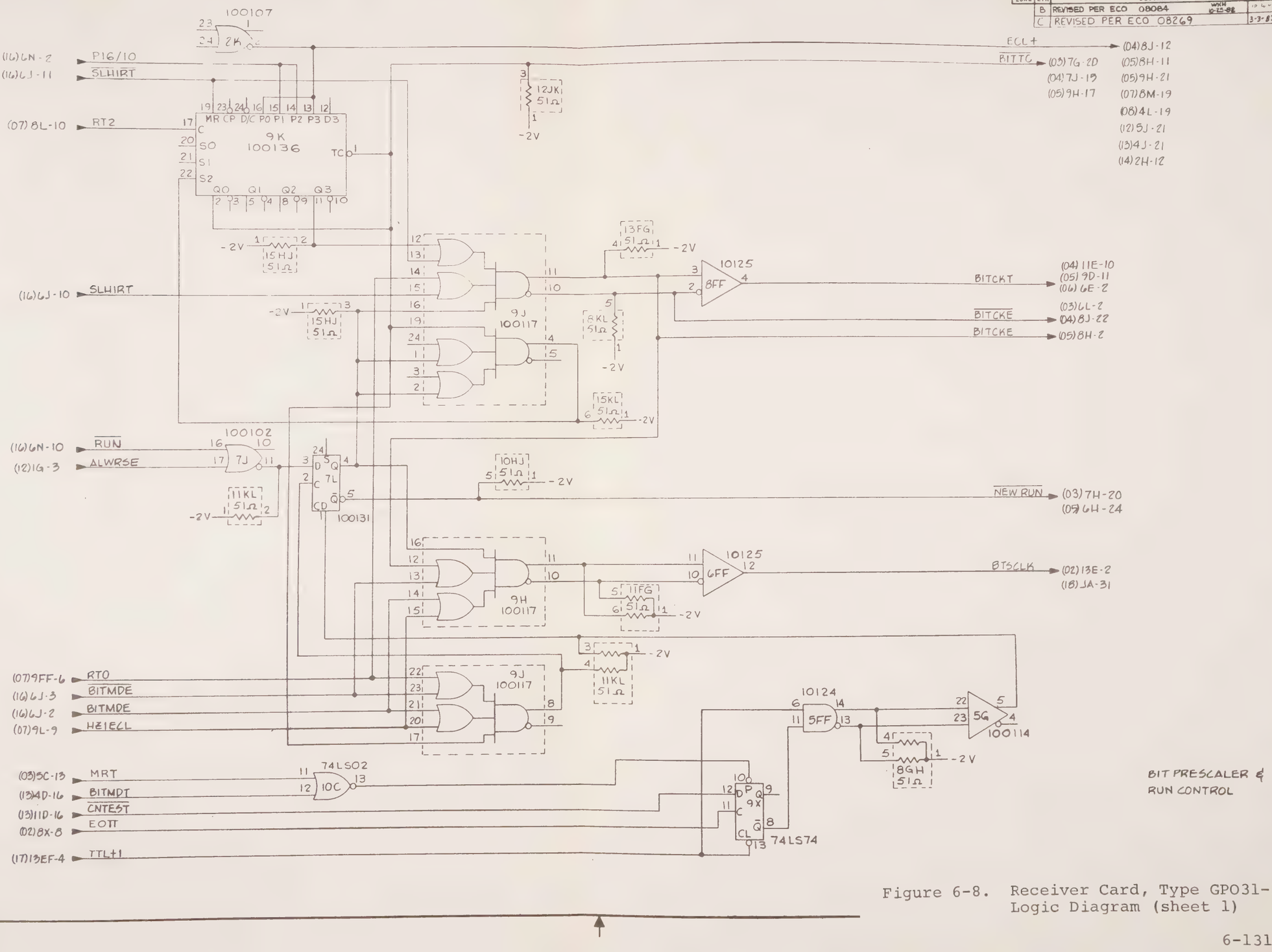


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 1)

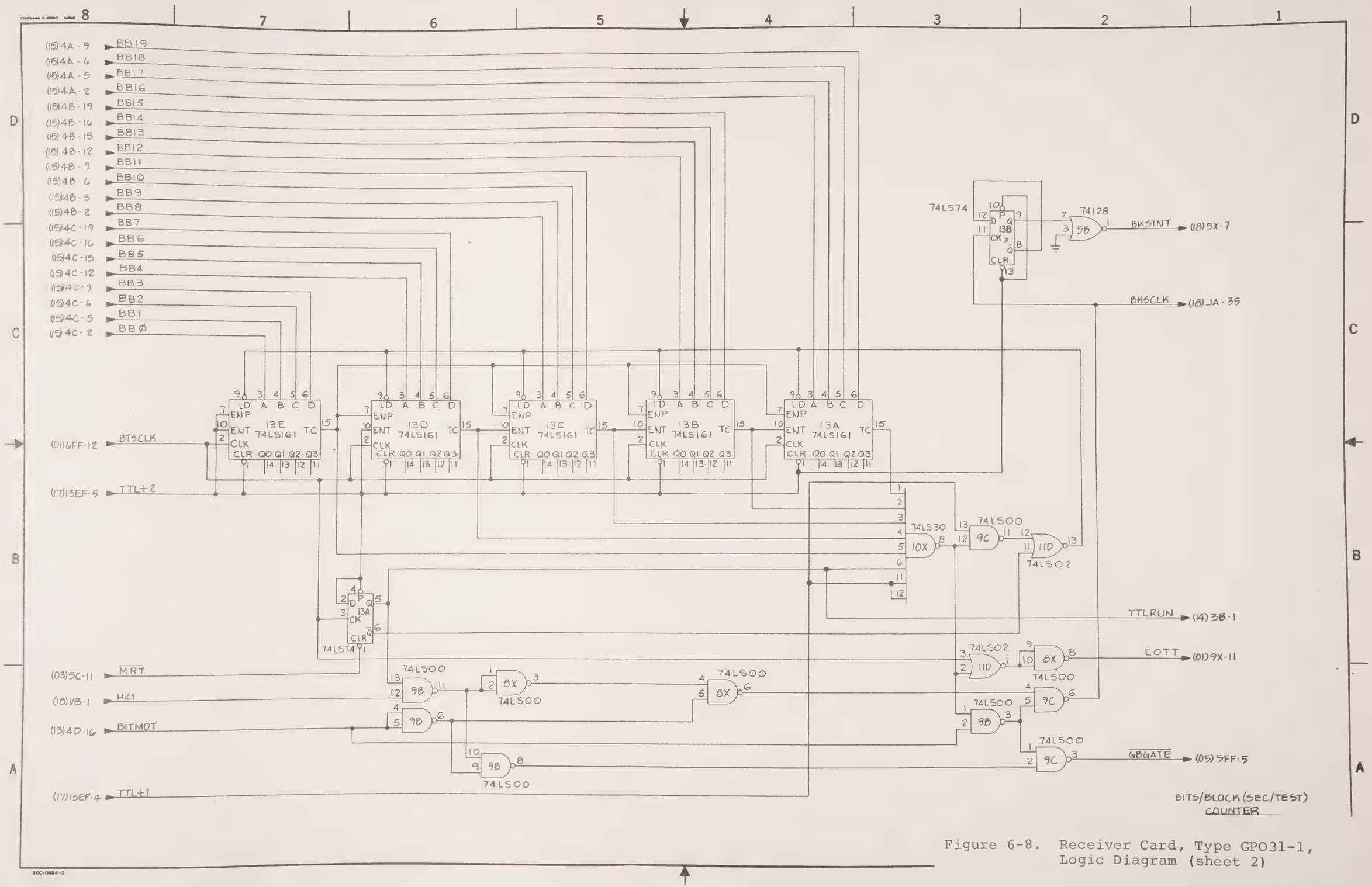


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 2)

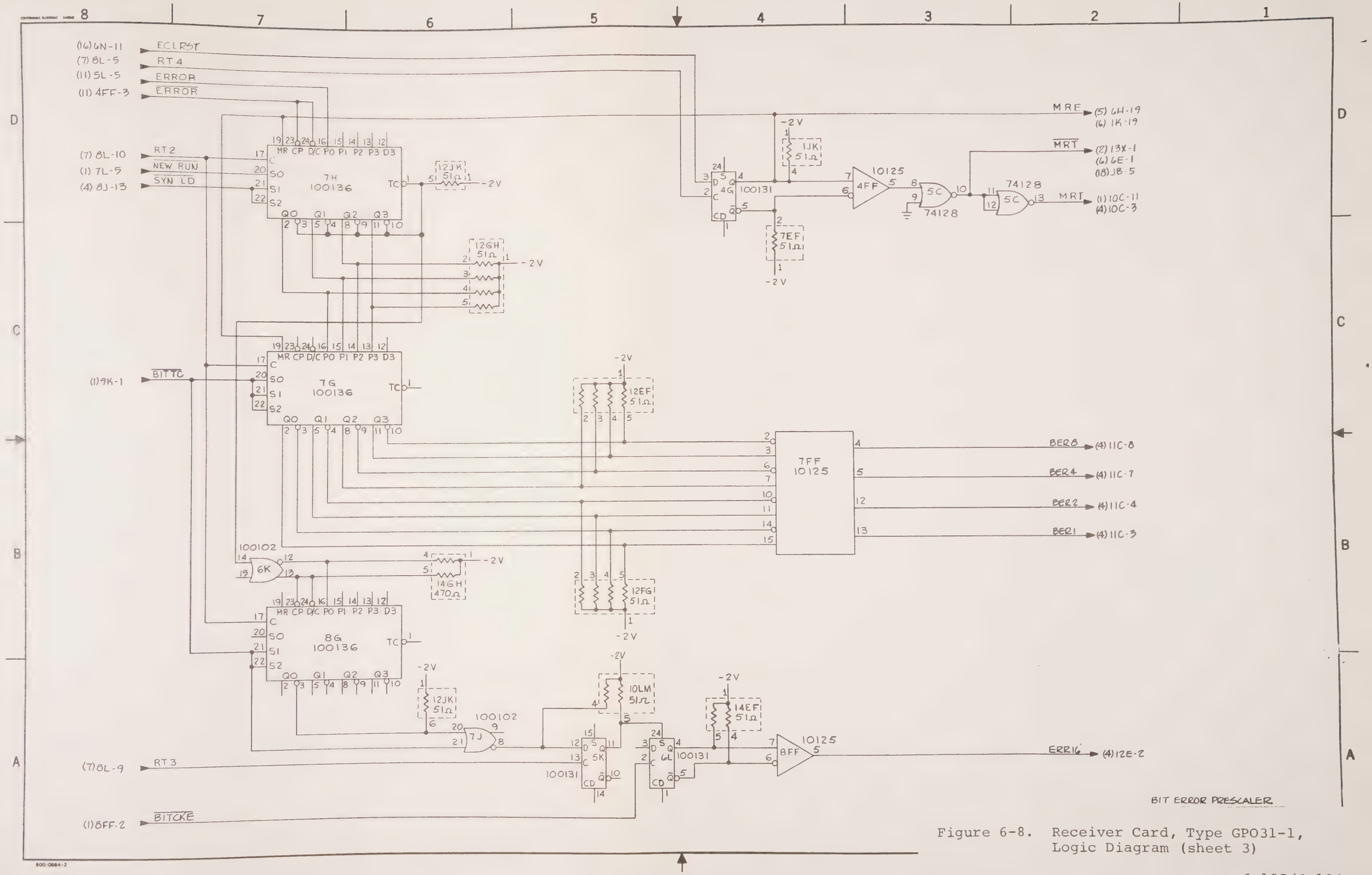


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 3)

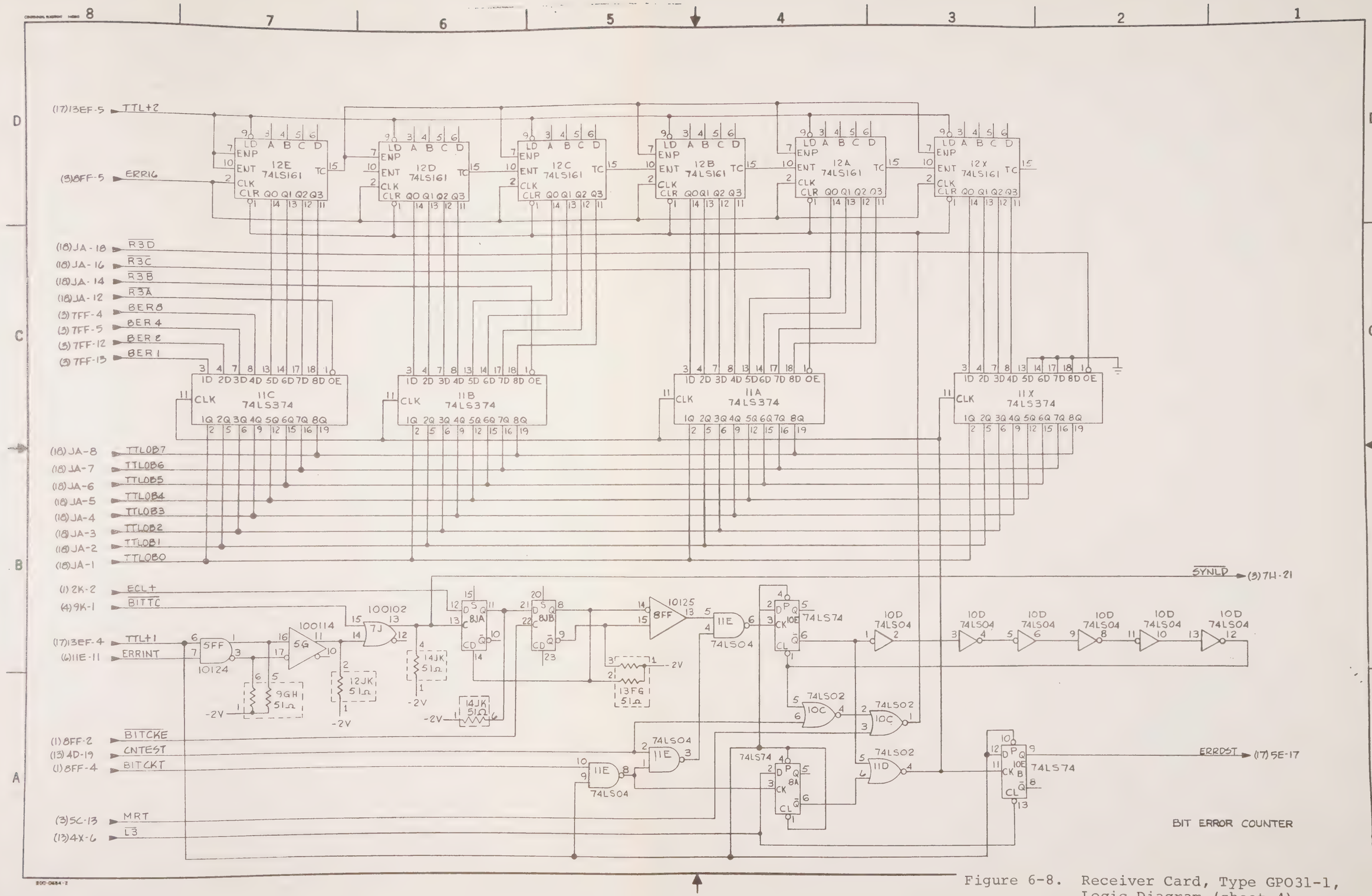


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 4)

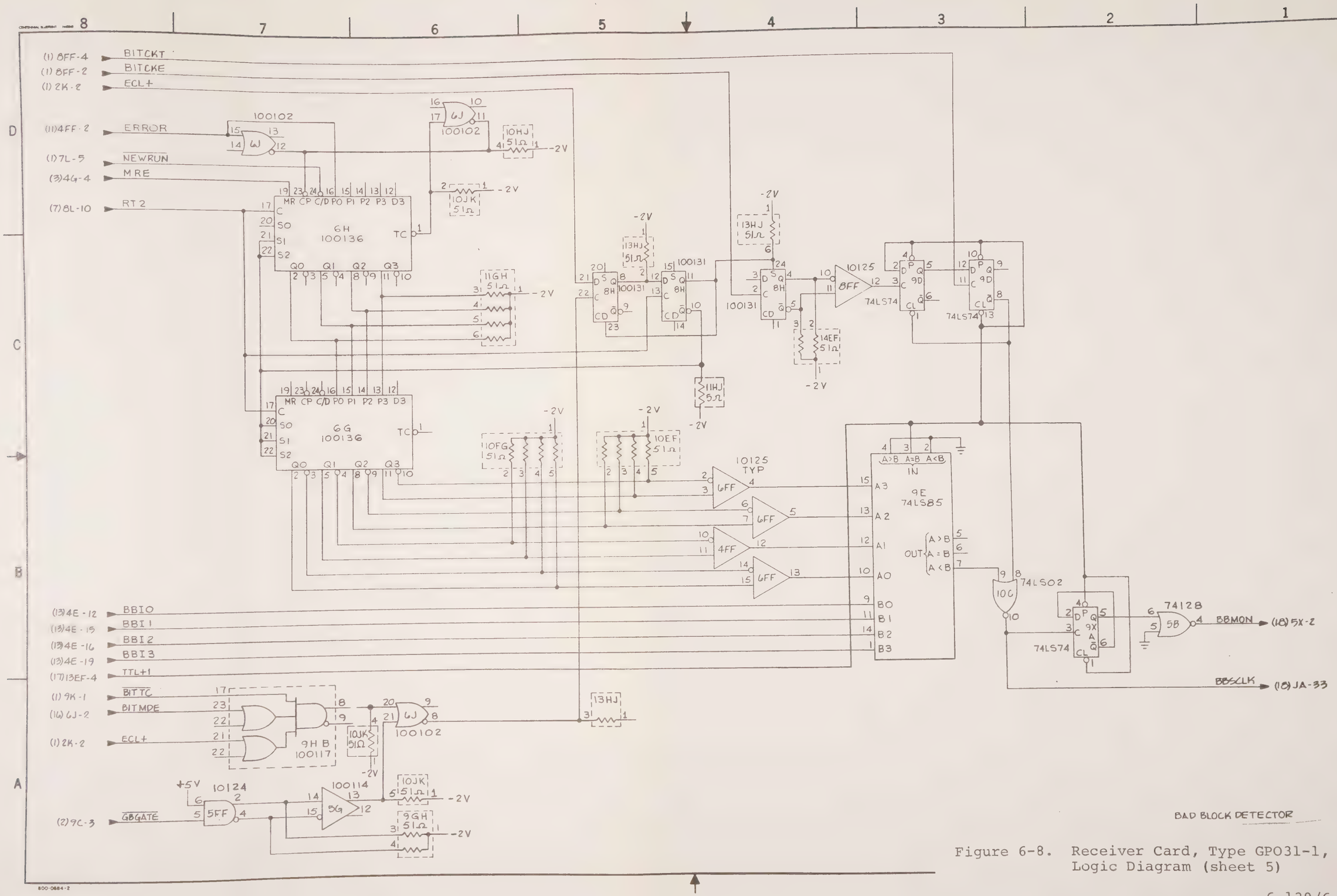


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 5)

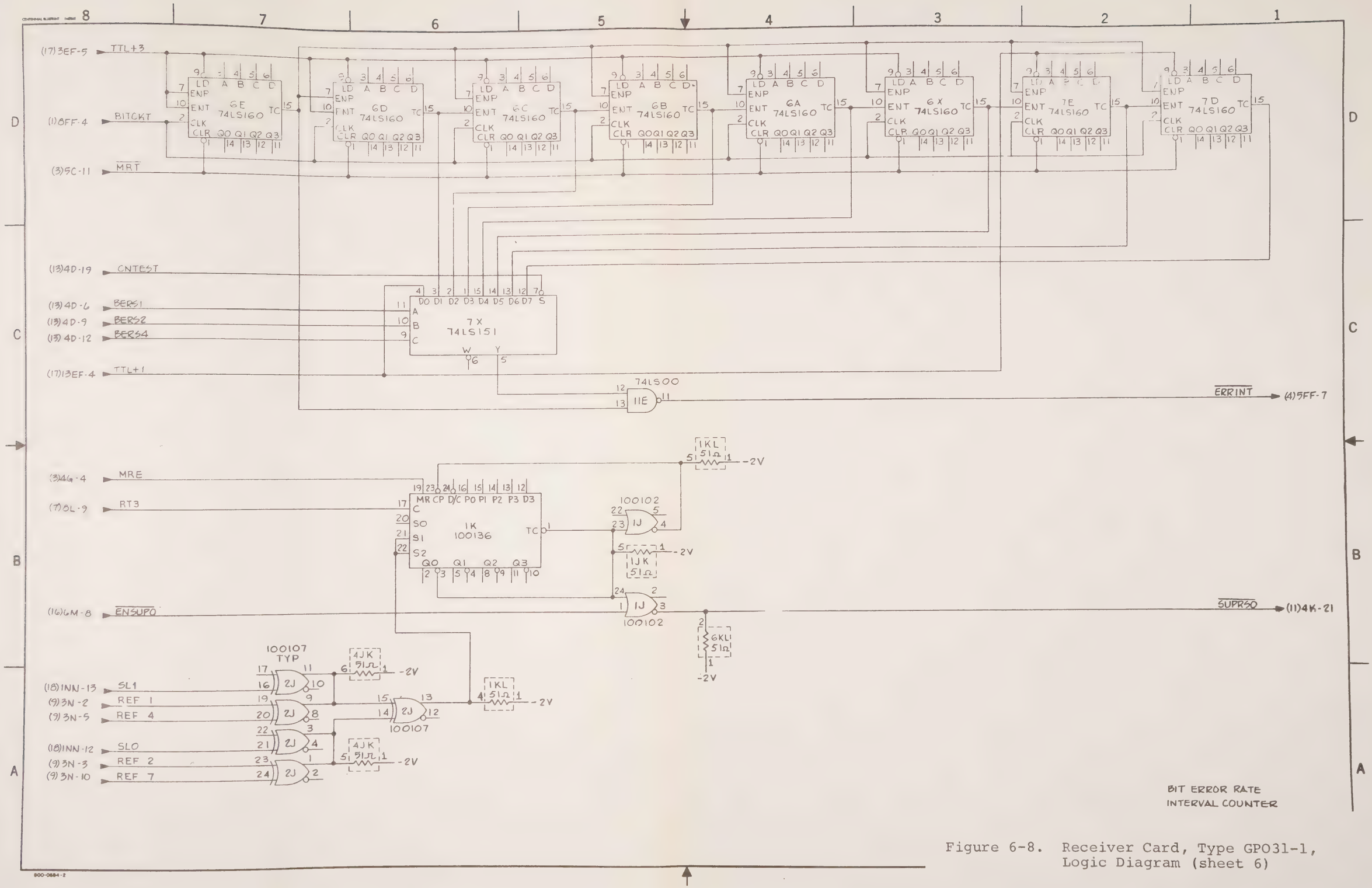


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 6)

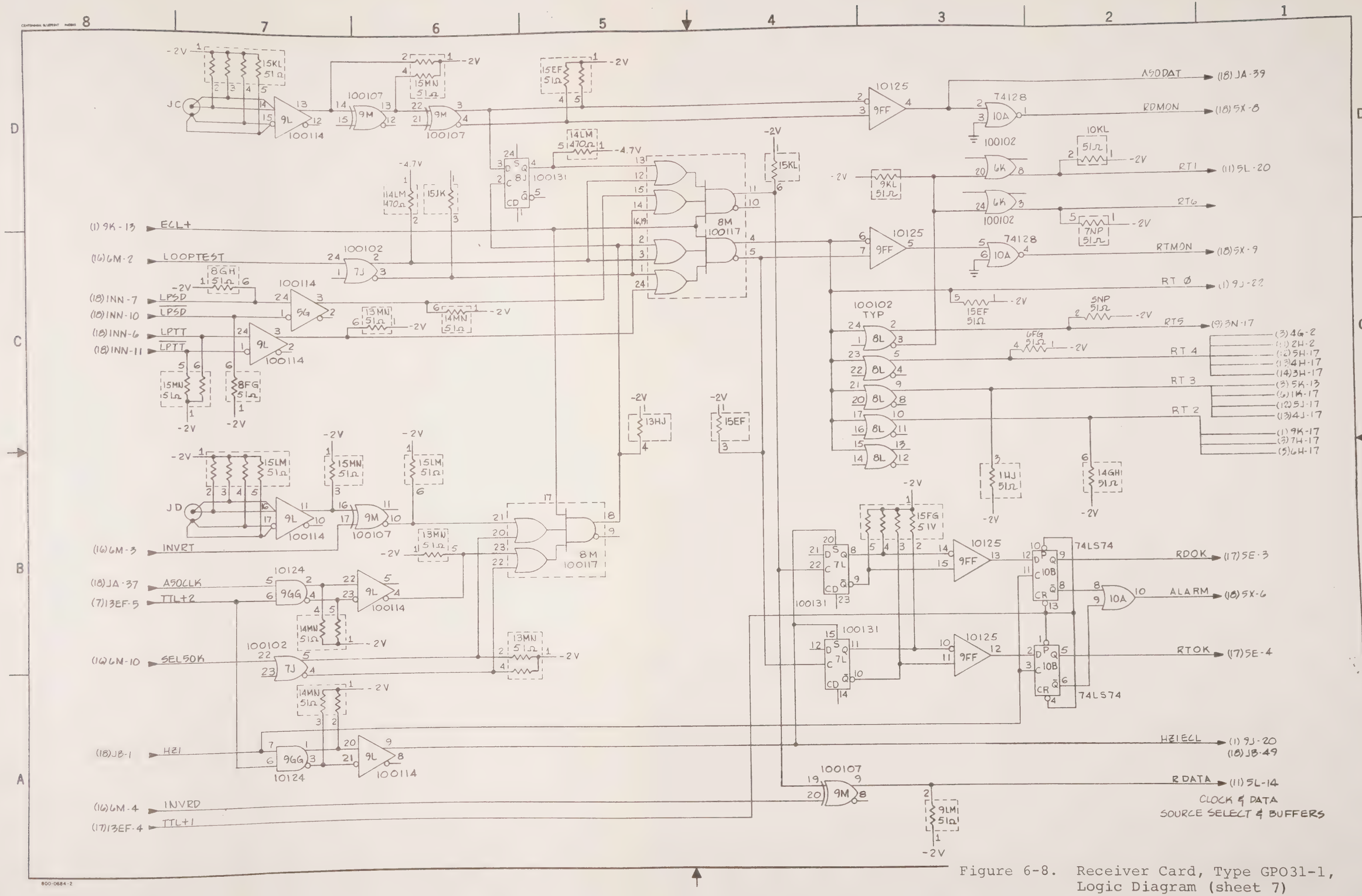


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 7)

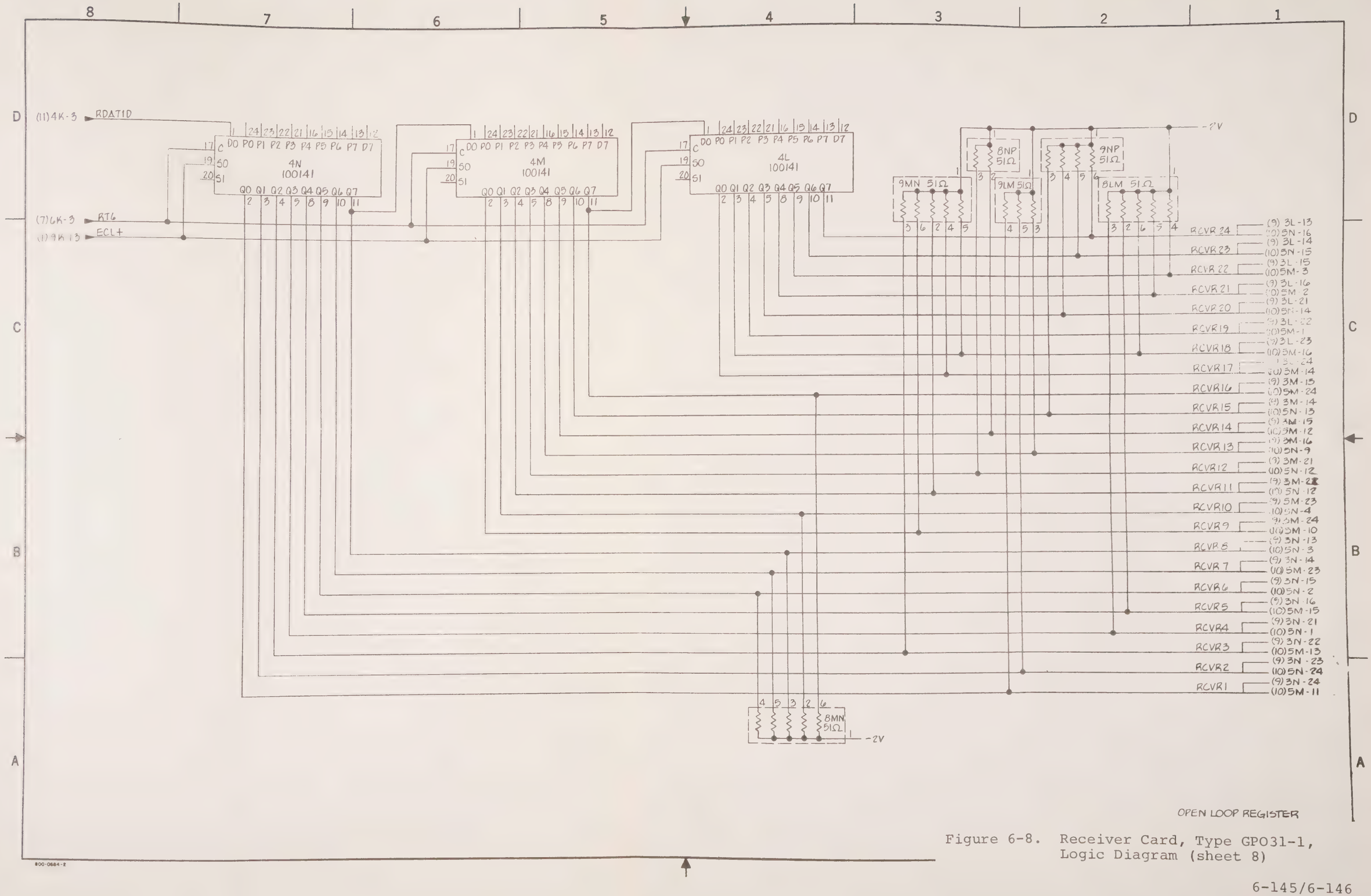


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 8)

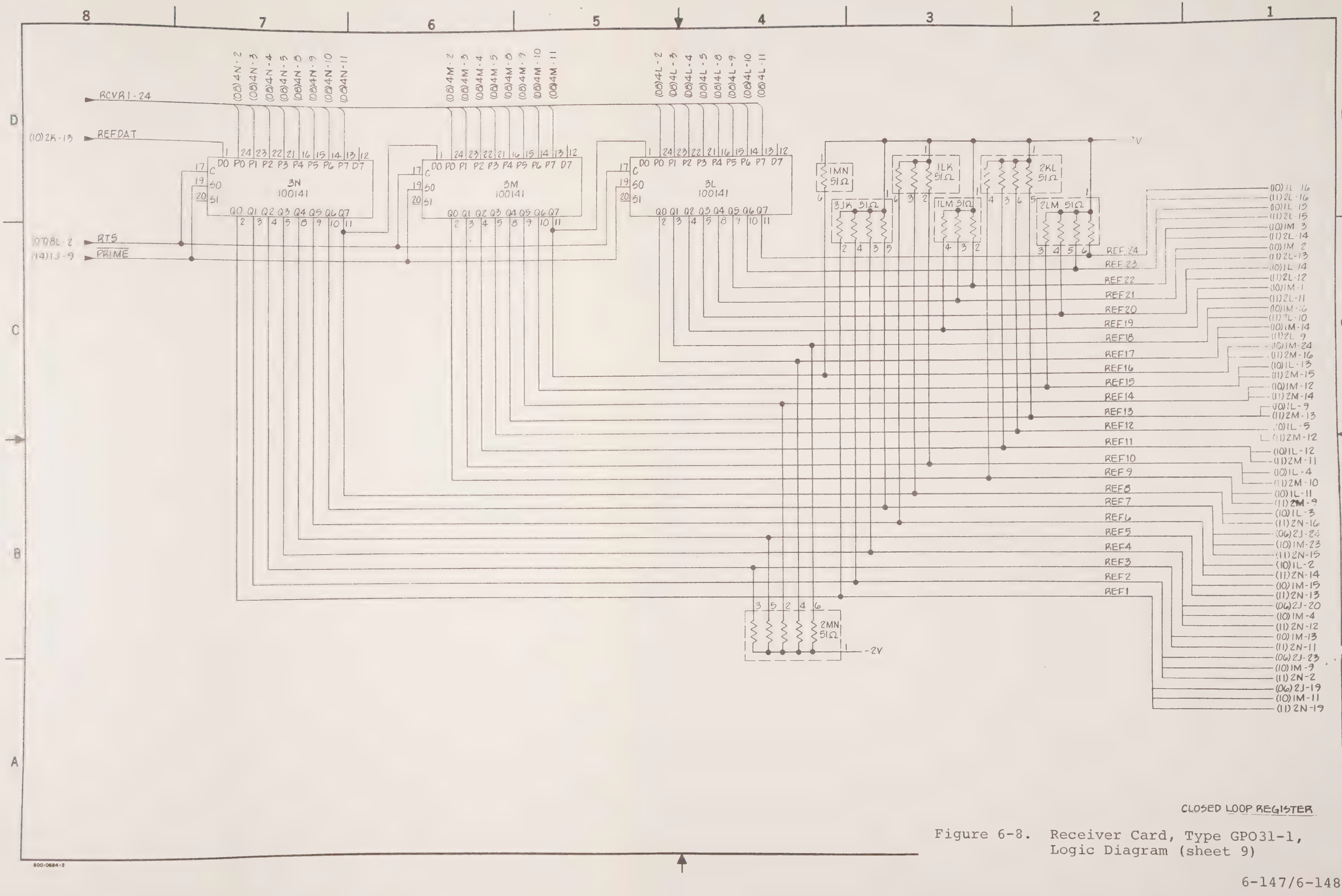


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 9)

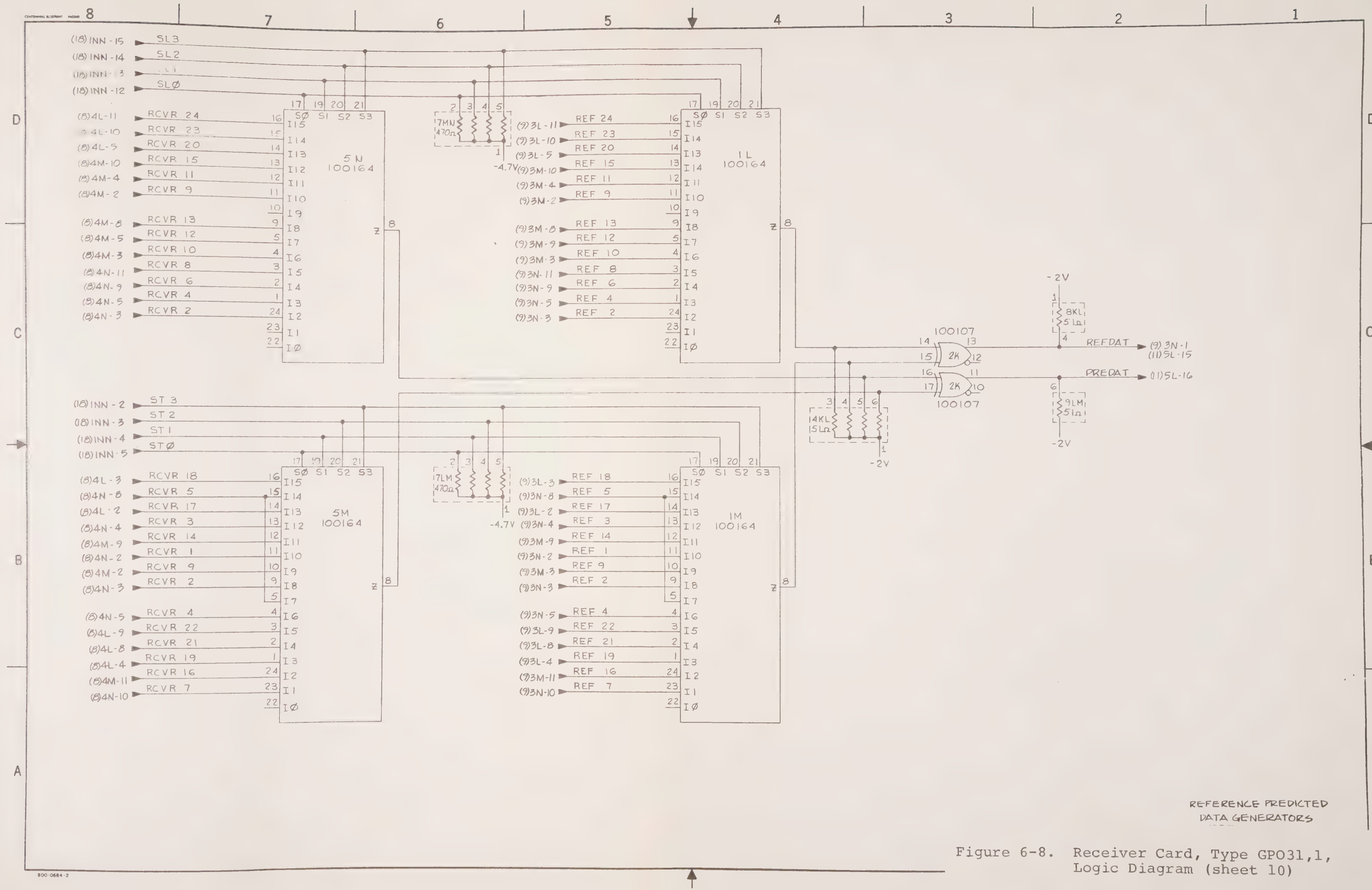


Figure 6-8. Receiver Card, Type GPO31,1, Logic Diagram (sheet 10)

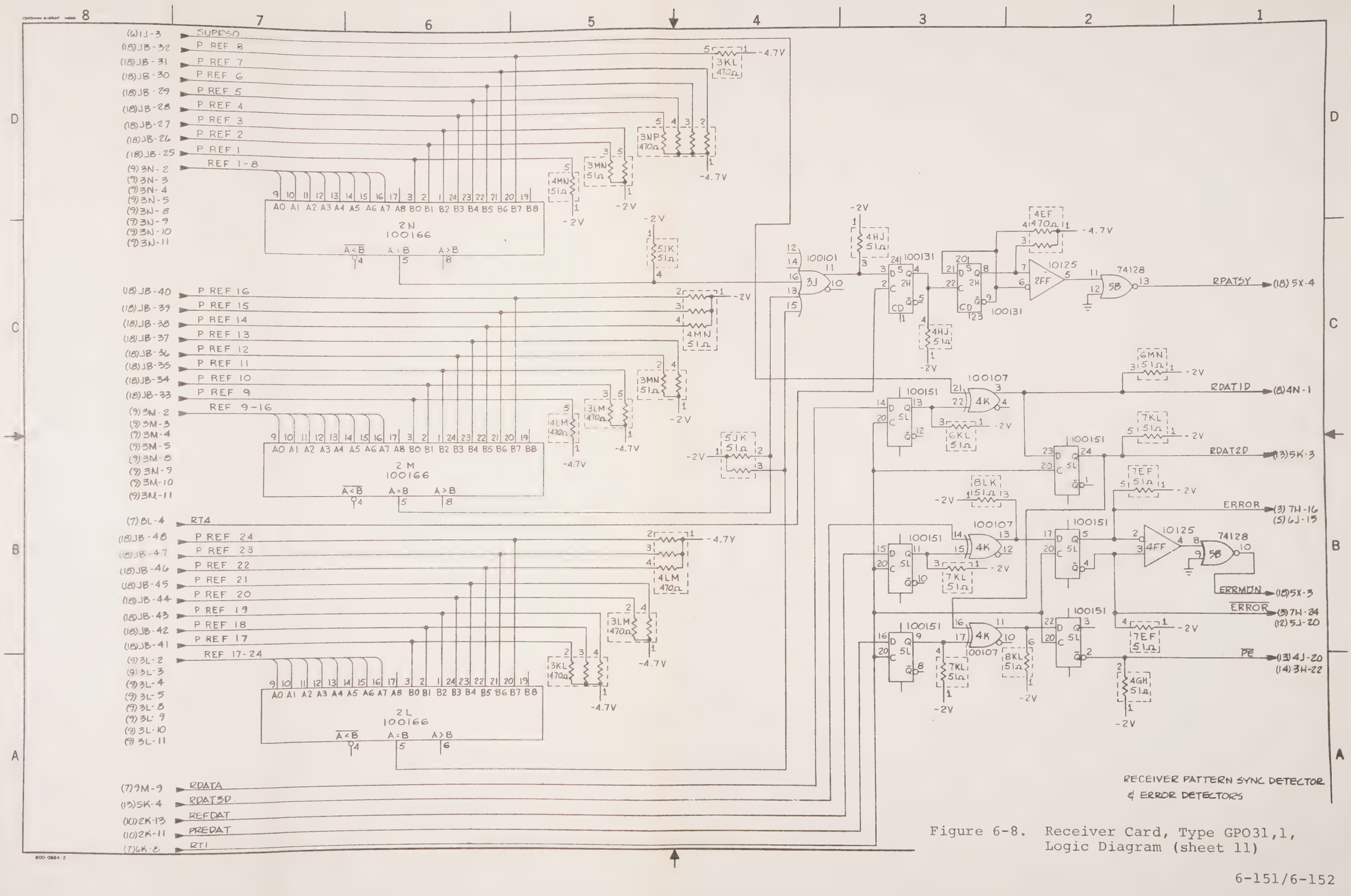


Figure 6-8. Receiver Card, Type GP031,1, Logic Diagram (sheet 11)

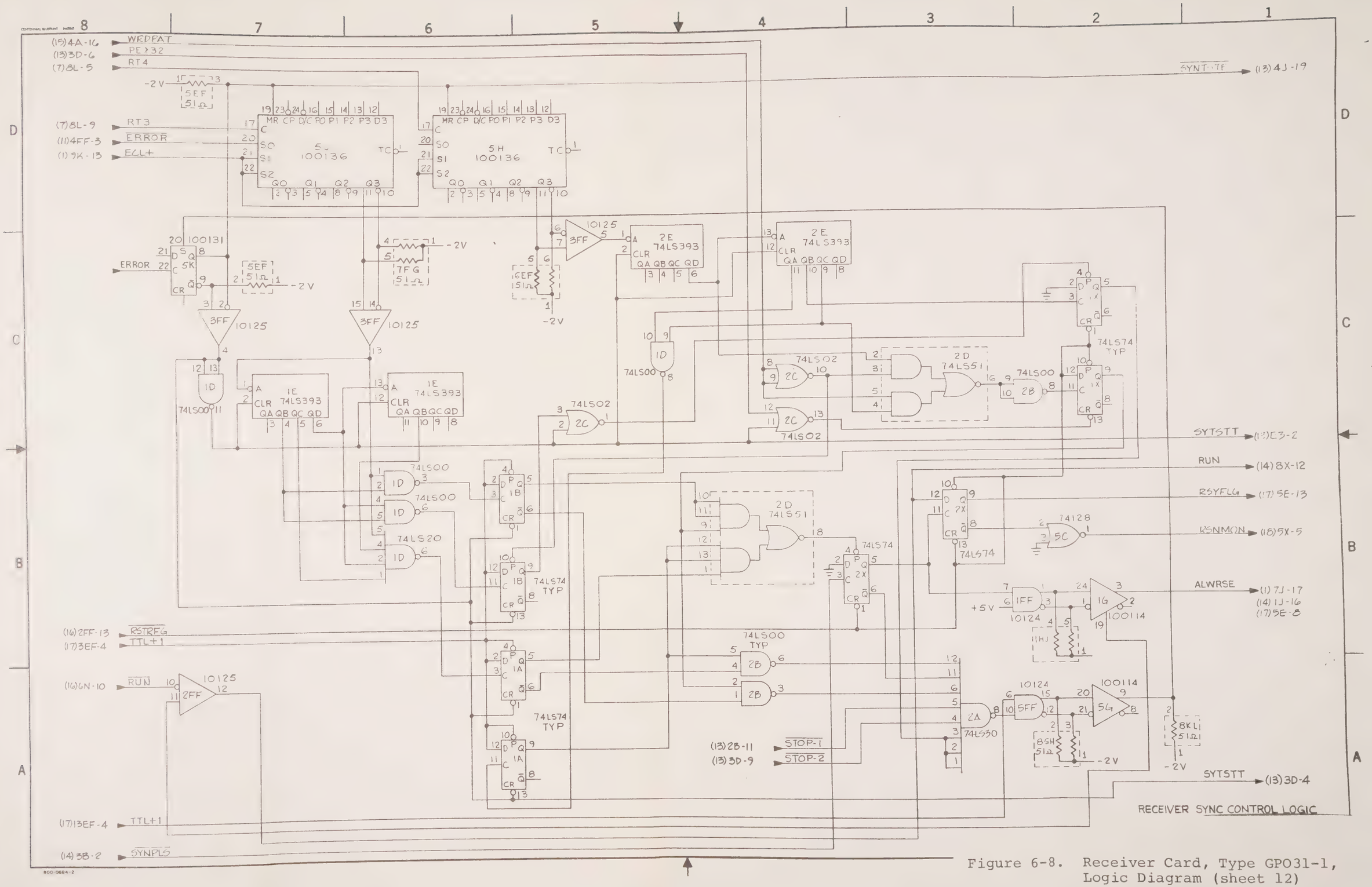


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 12)

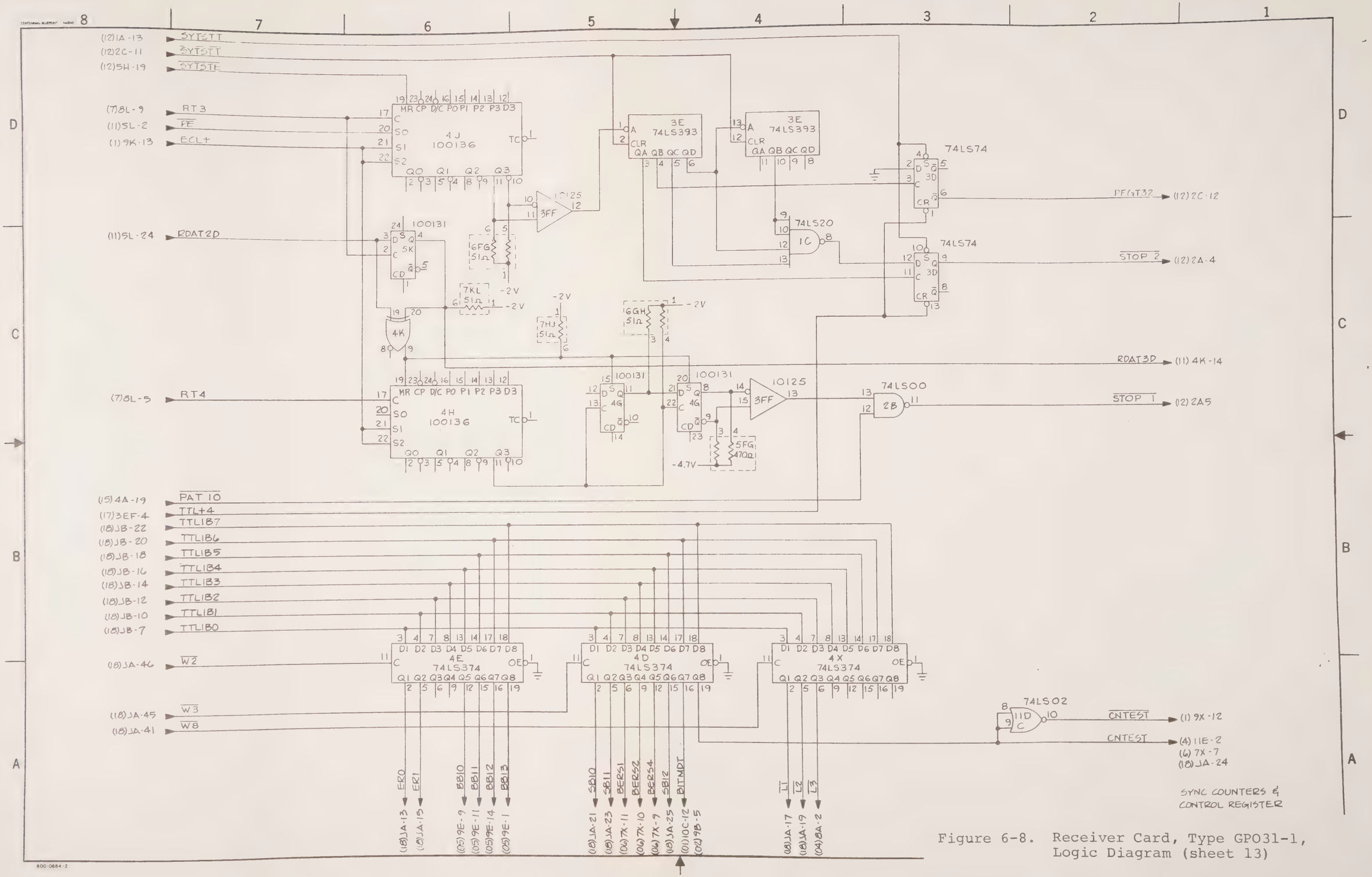


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 13)

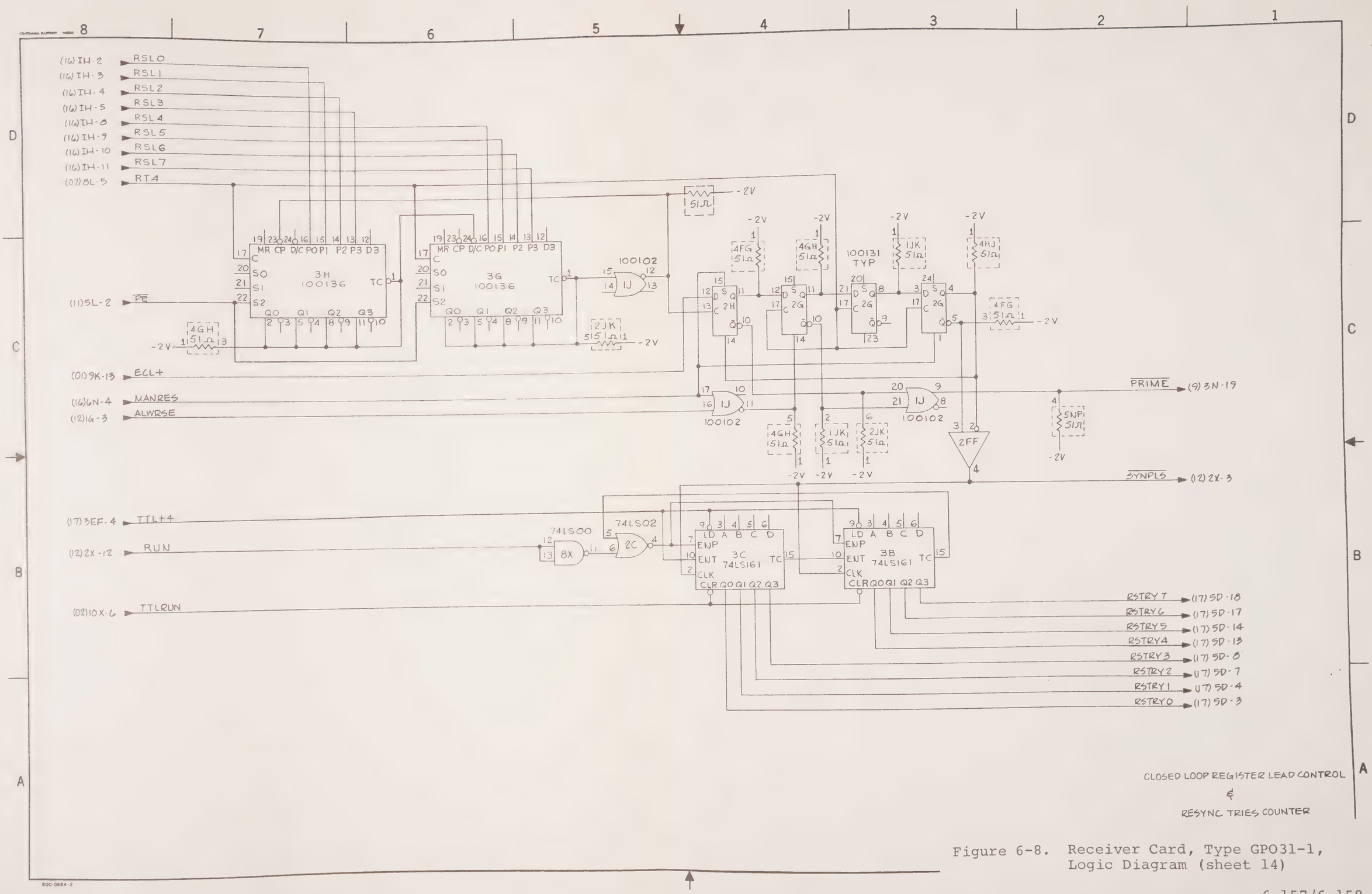


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 14)

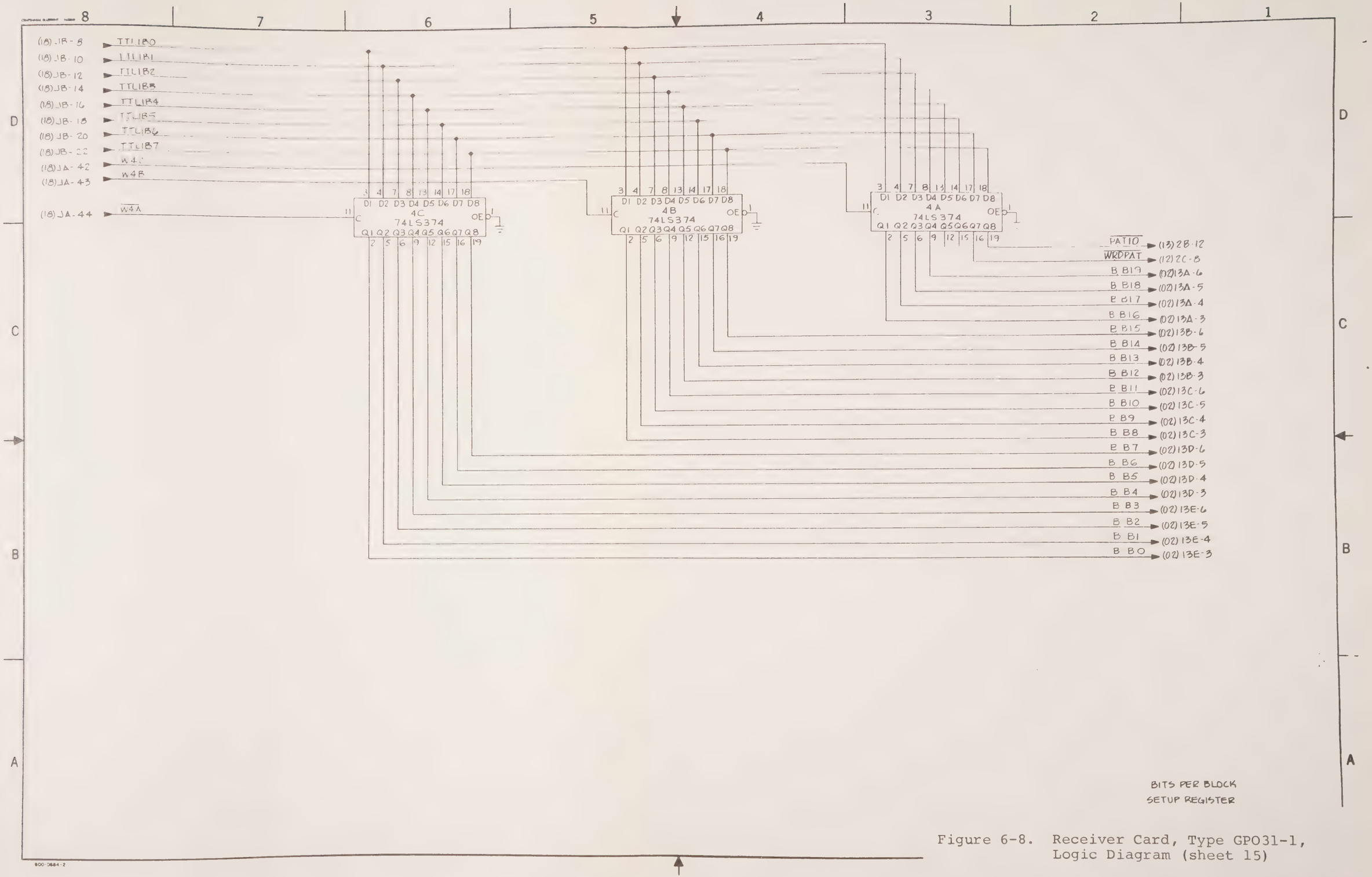


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 15)

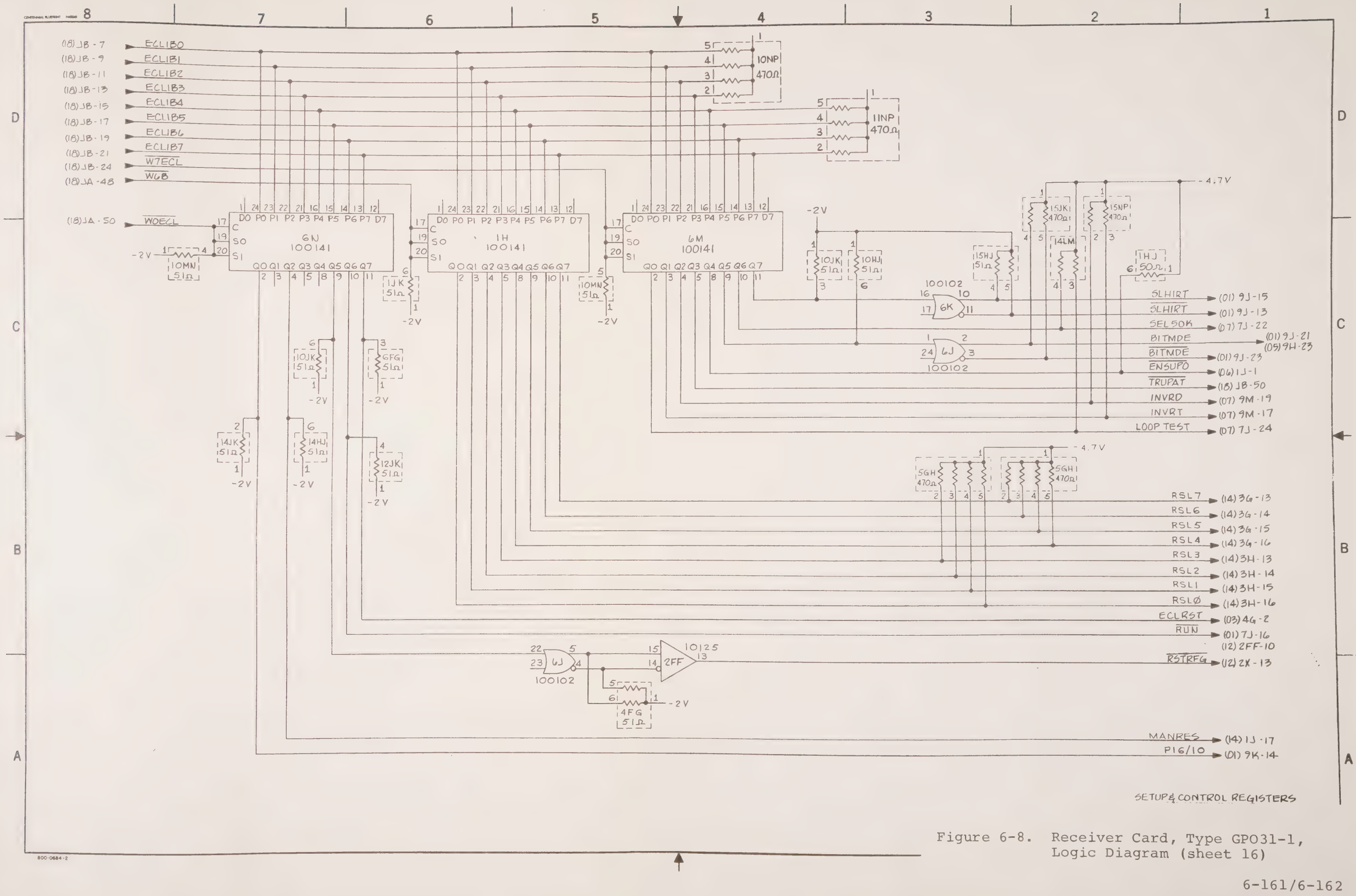


Figure 6-8. Receiver Card, Type GP031-1, Logic Diagram (sheet 16)

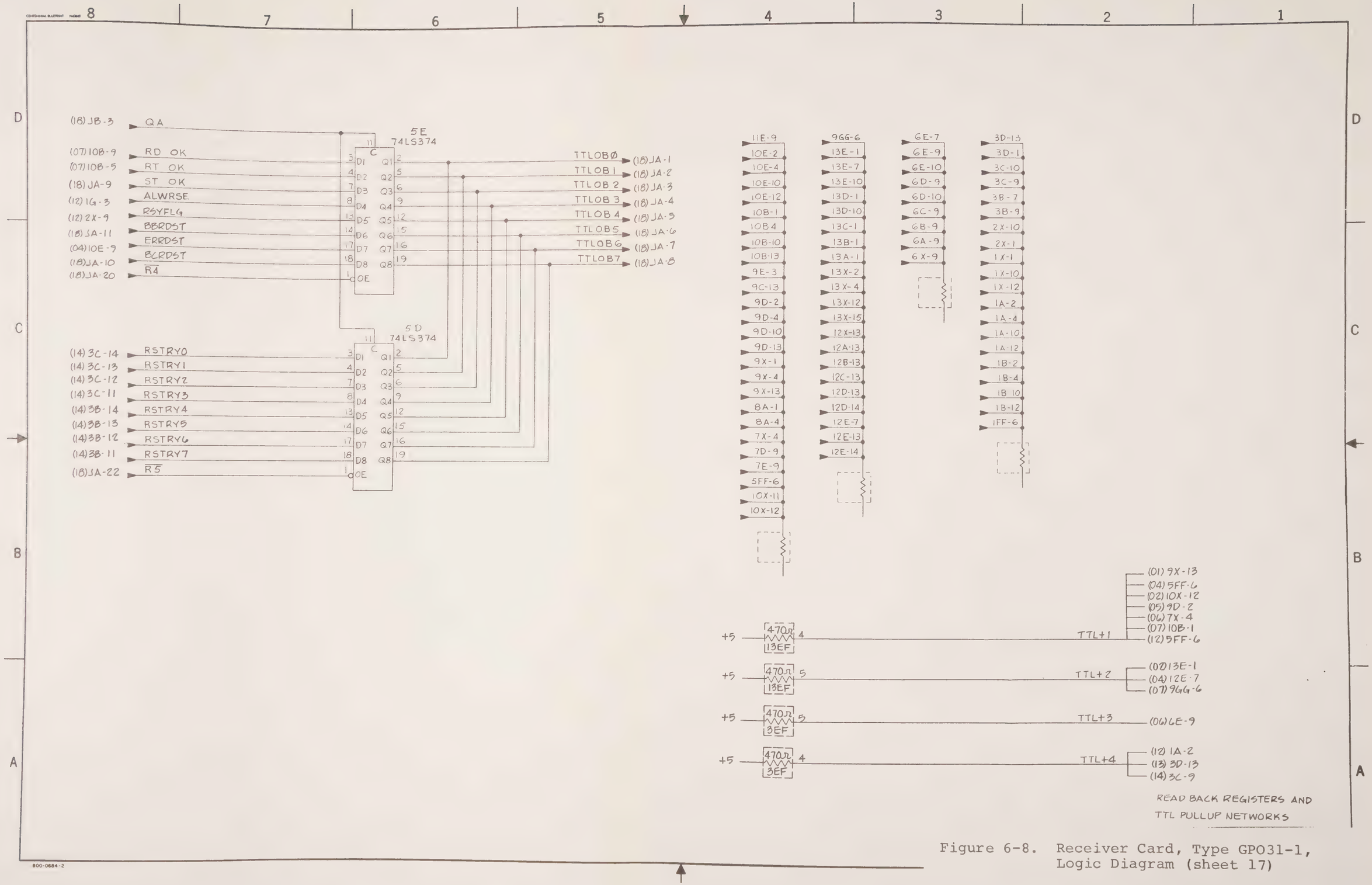


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 17)

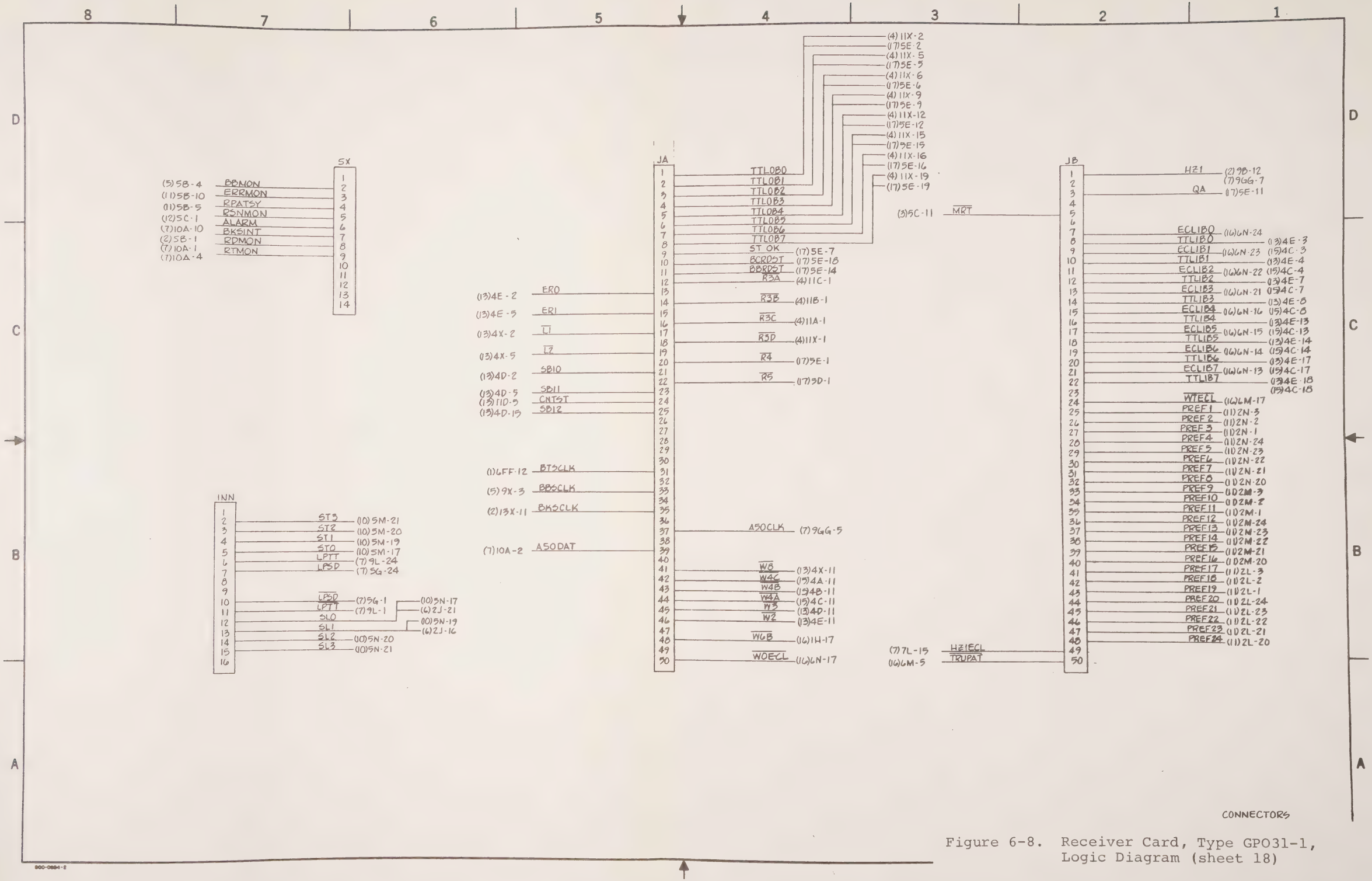
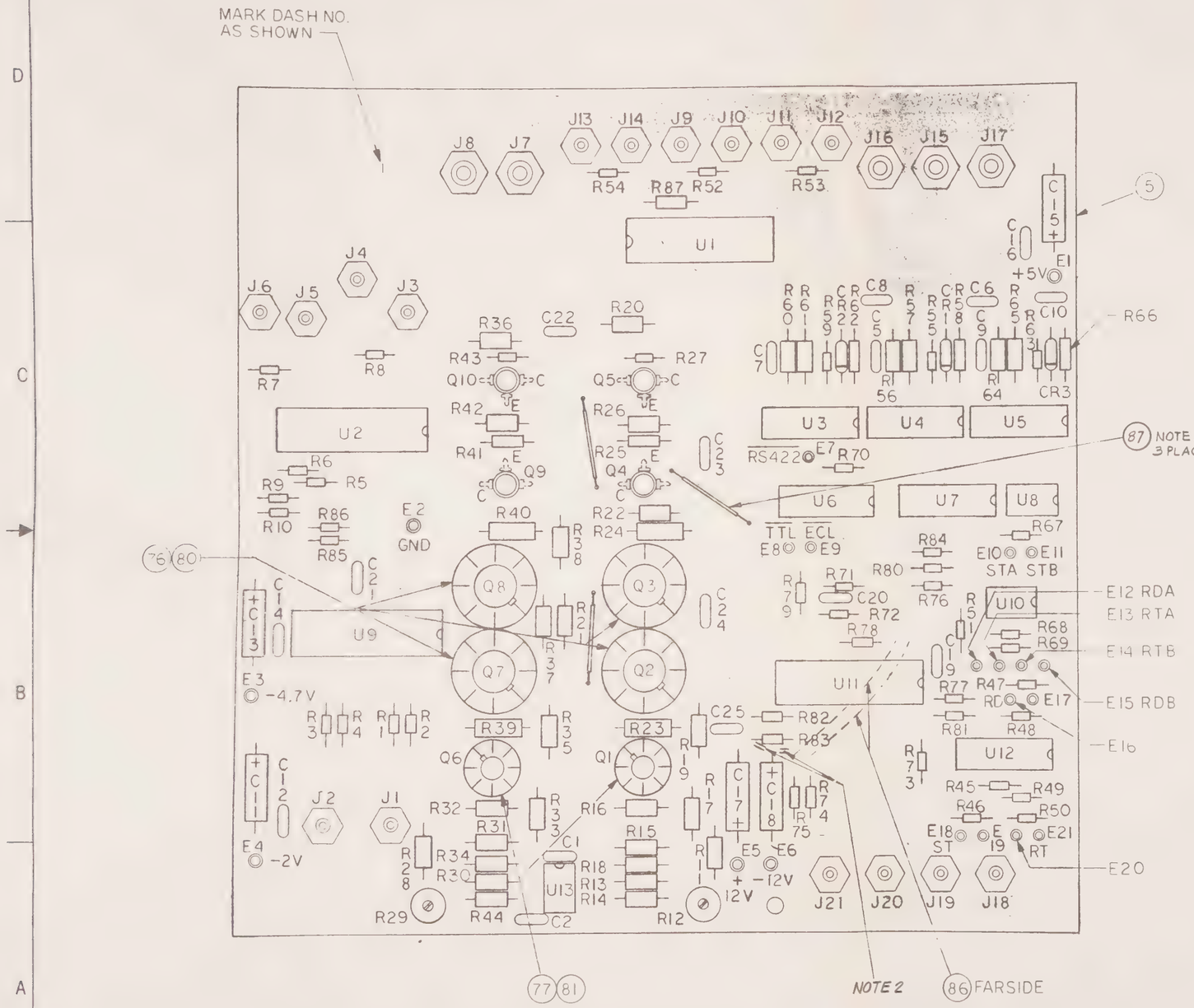


Figure 6-8. Receiver Card, Type GPO31-1, Logic Diagram (sheet 18)

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	C	REVISED PER ECO 06503 A KANE 7-20-81	7-20-81	
	D	REVISED PER ECO 07371 RPR REMARKS	9-2-82	
	E	REVISED PER ECO 08084 WKM 9 20 82		



NOTES:

1. FOR GENERAL MANUFACTURING AND ENGINEERING NOTES SEE DWG NO. 401-0010.
2. CUT GROUND PATTERNS WHERE SHOWN.
3. ADD LAP JOINT JUMPERING GROUND PLANES WHERE SHOWN

FOR PARTS LIST SEE PL 460-1658-501

800 0684 1A

Figure 6-9. Interface Card, Type INF014-1, Assembly and Schematic Diagram (sheet 1)

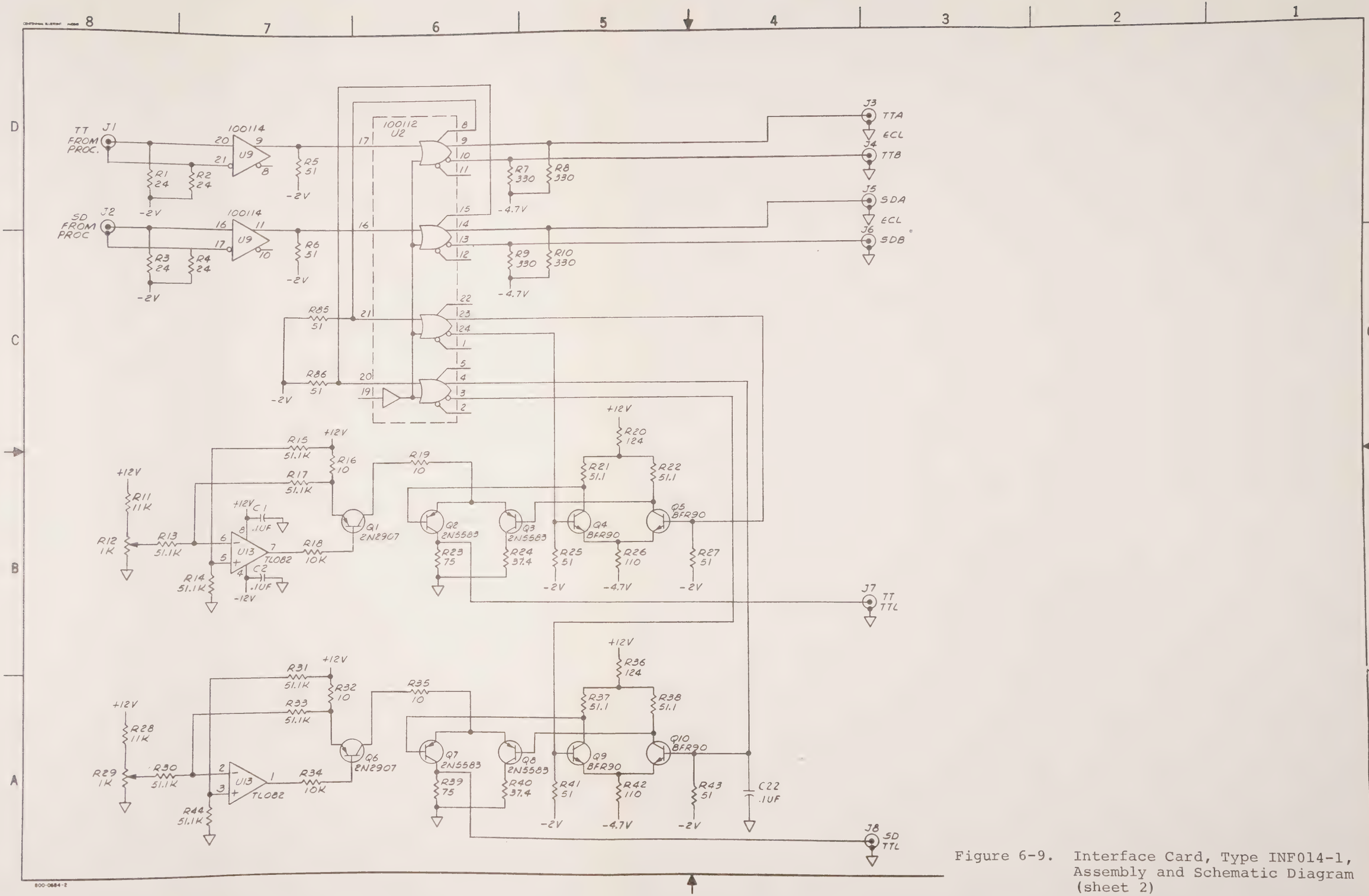


Figure 6-9. Interface Card, Type INF014-1, Assembly and Schematic Diagram (sheet 2)

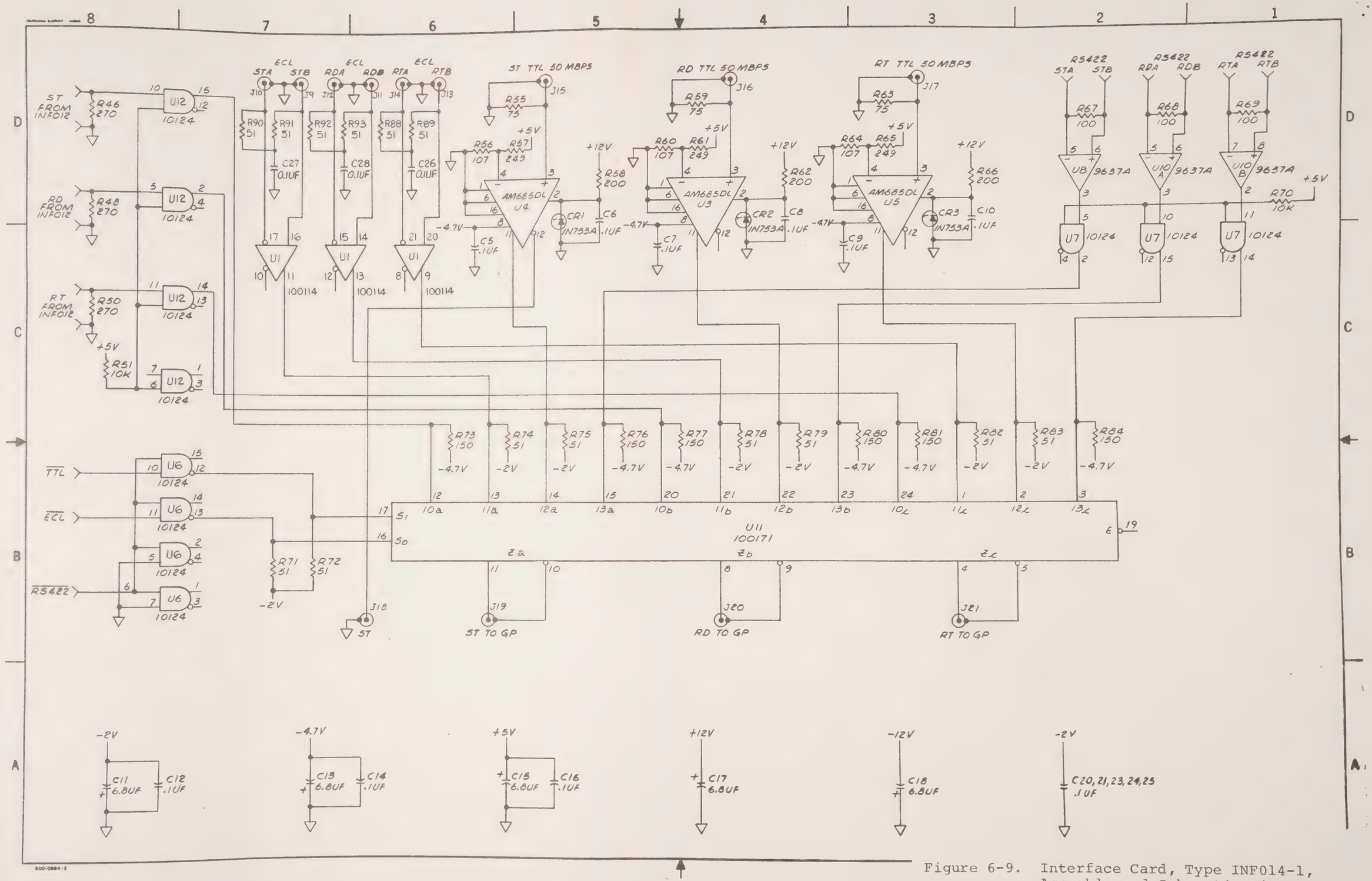


Figure 6-9. Interface Card, Type INF014-1, Assembly and Schematic Diagram (sheet 3)

Table 6-7

Parts List, INF014-1 Circuit Card Assy.

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		CIRCUIT CARD ASSY., INF014-1	20747	460-1658-501	REF
C1,C2, C5-C10	6-9	Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	71590	CY20C104M	18
C11		Capacitor, Fxd. Tantalum 6.8 uf, ±10%, 35 Vdcw	56289	150D685X9035B2	5
C12		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	71590	CY20C104M	REF
C13		Capacitor, Fxd. Tantalum 6.8 uf, ±10%, 35 Vdcw	56289	150D685X9035B2	REF
C14		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	71590	CY20C104M	REF
C15		Capacitor, Fxd. Tantalum 6.8 uf, ±10%, 35 Vdcw	56289	150D685X9035B2	REF
C16		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	71590	CY20C104M	REF
C17, C18		Capacitor Fxd. Tantalum 6.8 uf, ±10% 35 Vdcw	56289	150D685X9035B2	REF
C19 - C25		Capacitor, Fxd. Ceramic 0.1 uf, ±20%, 50 Vdcw	71590	CY20C104M	REF
CR1 - CR3		Diode, Zener	04713	1N753A	3
J1 - J6		Connector, 50 Ohm Coax Receptacle	98291	5-051-0000	16
J7, J8	6-9	Connector, 75 Ohm Coax Receptacle	98291	5-151-0000	5

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
J9 - J14	6-9	Connector, 50 Ohm Coax Receptacle	98291	5-051-0000	REF
J15 - J17		Connector, 75 Ohm Coax Receptacle	98291	5-151-0000	REF
J18 - J21		Connector, 50 Ohm Coax Receptacle	98291	5-051-0000	REF
Q1		Transistor, Silicon PNP	04713	2N2907	2
		Heatsink, TO-18	98978	TXBF-019-025B	2
		Transpad	07047	10047	2
Q2, Q3		Transistor, Silicon PNP	04713	2N5583	4
		Heatsink, TO-5	98978	TXBF-032-025B	4
		Transpad	07047	10030	4
Q4, Q5		Transistor, Silicon NPN	04713	BFR90	4
Q6		Transistor, Silicon PNP	04713	2N2907	REF
		Heatsink, TO-18	98978	TXBF-019-025B	REF
		Transpad	07047	10047	REF
Q7, Q8		Transistor, Silicon PNP	04713	2N5583	REF
		Heatsink, TO-5	98978	TXBF-032-025B	REF
		Transpad	07047	10030	REF
Q9, Q10	6-9	Transistor, Silicon NPN	04713	BFR90	REF

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R1 - R4	6-9	Resistor, Fxd. Composition 24 Ohms, ±5%, 1/8 WATT	81349	RC05GF240J	4
R5, R6		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	16
R7 - R10		Resistor, Fxd. Composition 330 Ohms, ±5%, 1/8 WATT	81349	RC05GF331J	4
R11		Resistor, Fxd. Film 11K, ±1%, 1/8 WATT	81349	RN55D1102F	2
R12		Resistor, Variable Cermet 1K, ±10%, 1/2 WATT	80294	3339P-1-102	2
R13 - R15		Resistor, Fxd. Film 51.1K, ±1%, 1/8 WATT	81349	RN55D5112F	8
R16		Resistor, Fxd. Film 10 Ohms, ±1%, 1/8 WATT	81349	RN55D10ROF	4
R17		Resistor, Fxd. Film 51.1K, ±1%, 1/8 WATT	81349	RN55D5112F	REF
R18		Resistor, Fxd. Film 10K, ±1%, 1/8 WATT	81349	RN55D1002F	2
R19		Resistor, Fxd. Film 10 Ohms, ±1%, 1/8 WATT	81349	RN55D10R0F	REF
R20	6-9	Resistor, Fxd. Film 124 Ohms, ±1%, 1/8 WATT	81349	RN55D1240F	2

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R21, R22	6-9	Resistor, Fxd. Film 51.1 Ohms, ±1%, 1/8 WATT	81349	RN55D51R1F	4
R23		Resistor, Fxd. Film 75 Ohms, ±1%, 1/8 WATT	81349	RN60C75ROF	2
R24		Resistor, Fxd. Film 37.4 Ohms, ±1%, 1/8 WATT	81349	RN60C37R4F	2
R25		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R26		Resistor, Fxd. Film 110 Ohms, ±1%, 1/8 WATT	81349	RN55D1100F	2
R27		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R28		Resistor, Fxd. Film 11K, ±1%, 1/8 WATT	81349	RN55D1102F	REF
R29		Resistor, Variable Cermet 1K, ±10%, 1/2 WATT	80294	3339P-1-102	REF
R30, R31		Resistor, Fxd. Film 51.1K, ±1%, 1/8 WATT	81349	RN55D5112F	REF
R32		Resistor, Fxd. Film 10 Ohms, ±1%, 1/8 WATT	81349	RN55D10R0F	REF
R33	6-9	Resistor, Fxd. Film 51.1K, ±1%, 1/8 WATT	81349	RN55D5112F	REF

800-0566A

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R34	6-9	Resistor, Fxd. Film 10K, ±1%, 1/8 WATT	81349	RN55D1002F	REF
R35		Resistor, Fxd. Film 10 Ohms, ±1%, 1/8 WATT	81349	RN55D10R0F	REF
R36		Resistor, Fxd. Film 124 Ohms, ±1%, 1/8 WATT	81349	RN55D1240F	REF
R37, R38		Resistor, Fxd. Film 51.1 Ohms, ±1%, 1/8 WATT	81349	RN55D51R1F	REF
R39		Resistor, Fxd. Film 75 Ohms, ±1%, 1/8 WATT	81349	RN60C75R0F	REF
R40		Resistor, Fxd. Film 37.4 Ohms, ±1%, 1/8 WATT	81349	RN60C37R4F	REF
R41		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510F	REF
R42		Resistor, Fxd. Film 110 Ohms, ±1%, 1/8 WATT	81349	RN55D1100F	REF
R43		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R44		Resistor, Fxd. Film 51.1K, ±1%, 1/8 WATT	81349	RN55D5112F	REF
R45	6-9	Resistor, Fxd. Composition 180 Ohms, ±5%, 1/8 WATT	81349	RC05GF181J	3

Table 6-7

Parts List INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R46	6-9	Resistor, Fxd. Composition 270 Ohms, ±5%, 1/8 WATT	81349	RC05GF271J	3
R47		Resistor, Fxd. Composition 180 Ohms, ±5%, 1/8 WATT	81349	RC05GF181J	REF
R48		Resistor, Fxd. Composition 270 Ohms, ±5%, 1/8 WATT	81349	RC05GF271J	REF
R49		Resistor, Fxd. Composition 180 Ohms, ±5%, 1/8 WATT	81349	RC05GF181J	REF
R50		Resistor, Fxd. Composition 270 Ohms, ±5%, 1/8 WATT	81349	RC05GF271J	REF
R51		Resistor, Fxd. Composition 10K, ±5%, 1/8 WATT	81349	RC05GF103J	2
R52 - R54		Resistor, Fxd. Composition 100 Ohms, ±5%, 1/8 WATT	81349	RC05GF101J	6
R55		Resistor, Fxd. Composition 75 Ohms, ±5%, 1/8 WATT	81349	RC05GF750J	3
R56		Resistor, Fxd. Film 107 Ohms, ±1%, 1/8 WATT	81349	RN55D1070F	3
R57		Resistor, Fxd. Film 249 Ohms, ±1%, 1/8 WATT	81349	RN55D2490F	3
R58	6-9	Resistor, Fxd. Composition 200 Ohms, ±5%, 1/4 WATT	81349	RC07GF201J	3

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R59	6-9	Resistor, Fxd. Composition 75 Ohms, ±5%, 1/8 WATT	81349	RC05GF750J	REF
R60		Resistor, Fxd. Film 107 Ohms, ±1%, 1/8 WATT	81349	RN55D1070F	REF
R61		Resistor, Fxd. Film 249 Ohms, ±1%, 1/8 WATT	81349	RN55D2490F	REF
R62		Resistor, Fxd. Composition 200 Ohms, ±5%, 1/4 WATT	81349	RC07GF201J	REF
R63		Resistor, Fxd. Composition 75 Ohms, ±5%, 1/8 WATT	81349	RC05GF750J	REF
R64		Resistor, Fxd. Film 107 Ohms, ±1%, 1/8 WATT	81349	RN55D1070F	REF
R65		Resistor, Fxd. Film 249 Ohms, ±1%, 1/8 WATT	81349	RN55D2490F	REF
R66		Resistor, Fxd. Composition 200 Ohms, ±5%, 1/4 WATT	81349	RC07GF201J	REF
R67 - R69		Resistor, Fxd. Composition 100 Ohms, ±5%, 1/8 WATT	81349	RC05GF101J	REF
R70		Resistor, Fxd. Composition 10K, ±5%, 1/8 WATT	81349	RC05GF103J	REF
R71, R72	6-9	Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF

Table 6-7

Parts List INF014-1 Circuit Card Assy. (cont.)

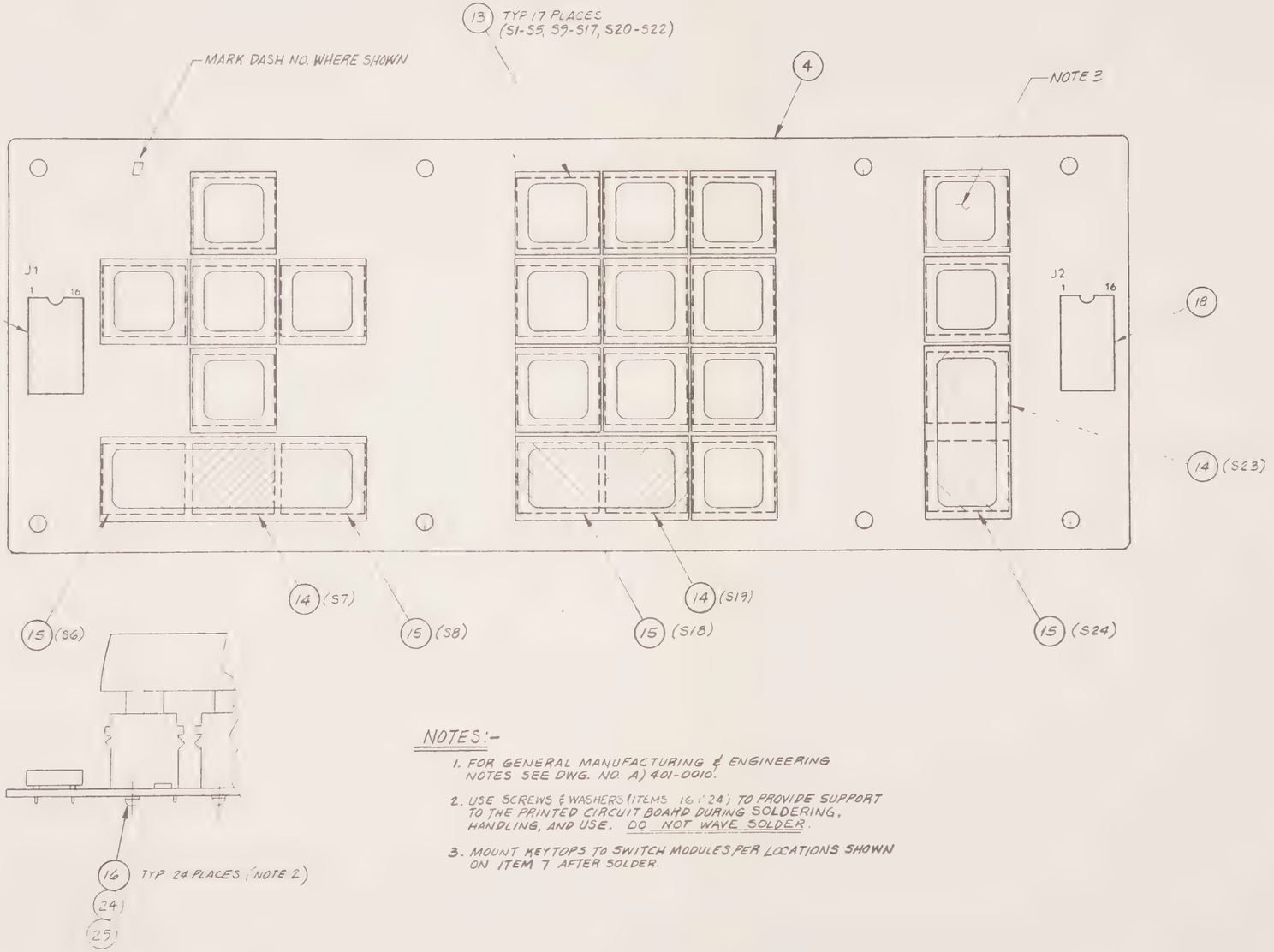
Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
R73	6-9	Resistor, Fxd. Composition 150 Ohms, ±5%, 1/8 WATT	81349	RC05GF151J	6
R74, R75		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R76, R77		Resistor, Fxd. Composition 150 Ohms, ±5%, 1/8 WATT	81349	RC05GF151J	REF
R78, R79		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R80, R81		Resistor, Fxd. Composition 150 Ohms, ±5%, 1/8 WATT	81349	RC05GF151J	REF
R82, R83		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R84		Resistor, Fxd. Composition 150 Ohms, ±5%, 1/8 WATT	81349	RC05GF151J	REF
R85, R86		Resistor, Fxd. Composition 51 Ohms, ±5%, 1/8 WATT	81349	RC05GF510J	REF
R87		Resistor, Fxd. Composition 120 Ohms, ±5%, 1/4 WATT	81349	RC07GF121J	1
U1		Integrated Circuit, ECL Line Receiver	07263	F100114DC	2
U2	6-9	Integrated Circuit, ECL Driver	07263	F100112DC	1

Table 6-7

Parts List, INF014-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
U3 - U5	6-9	Integrated Circuit Voltage Comparator	34335	AM685DL	3
U6, U7		Integrated Circuit, ECL TTL to ECL Translator	07263	F10124PC	3
U8		Integrated Circuit Differential Line Receiver	07263	9637ATC	2
U9		Integrated Circuit, ECL Line Receiver	07263	F100114DC	REF
U10		Integrated Circuit Differential Line Receiver	07263	9637ATC	REF
U11		Integrated Circuit, ECL 1 of 4 Decoder/Demultiplexer	07263	F100171DC	1
U12		Integrated Circuit, ECL TTL to ECL Translator	07263	F10124PC	REF
U13		Integrated Circuit Operational Amplifier	01295	TL082CP	1
	6-9	Printed Wiring Board	20747	400-1745	1

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO C5519	7-7-80	
	C	REVISED PER ECO 06032		
	D	REVISED PER ECO 06125		
	E	REVISED PER ECO 07482	4 21 82	DBC



NOTES:-

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. NO. A) 401-0010.
2. USE SCREWS & WASHERS (ITEMS 16 & 24) TO PROVIDE SUPPORT TO THE PRINTED CIRCUIT BOARD DURING SOLDERING, HANDLING, AND USE. DO NOT WAVE SOLDER.
3. MOUNT KEYTOPS TO SWITCH MODULES PER LOCATIONS SHOWN ON ITEM 7 AFTER SOLDER.

FOR PARTS LIST SEE PL 460-1678-□

800-0684-1

Figure 6-10. Front Panel Keyboard Card, Type FPK001-1, Assembly Drawing

Table 6-8

Parts List, FPK001-1 Circuit Card Assy.

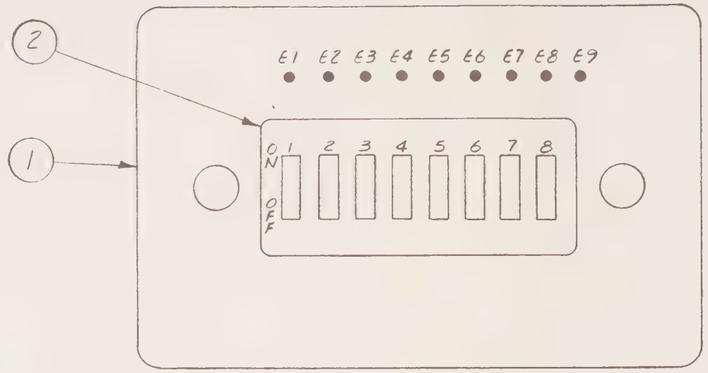
Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
		CIRCUIT CARD ASSY., FPK001-1	20747	460-1678-501	REF
J1, J2	6-10	Socket, 16 Pin Integrated Circuit	91506	516-AG19D	2
S1 - S5		Switch, Solid State Momentary Sink Level, 2.50Z Operating Force	91929	1001SD-4-A-3-A	17
		Pushbutton, Modified	20747	177-015-001	1set
S6		Support, Switch	91929	1001SD-6-A-1-D	4
S7		Switch, Solid State Momentary Sink Level, 1.30Z Operating Force	91929	1001SD-4-A-1-A	3
		Pushbutton, Modified	20747	177-015-001	REF
S8		Support, Switch	91929	1001SD-6-A-1-D	REF
S9 - S17		Switch, Solid State Momentary Sink Level, 2.50Z Operating Force	91929	1001SD-4-A-3-A	REF
		Pushbutton, Modified	20747	177-015-001	REF
S18		Support, Switch	91929	1001SD-6-A-1-D	REF
S19		Switch, Solid State Momentary Sink Level, 1.30Z Operating Force	91929	1001SD-4-A-1-A	REF
		Pushbutton, Modified	20747	177-015-001	REF
S20 - S22		Switch, Solid State Momentary Sink Level, 2.50Z Operating Force	91929	1001SD-4-A-3-A	REF
		Pushbutton, Modified	20747	177-015-001	REF
S23	6-10	Switch, Solid State Momentary Sink Level, 1.30Z Operating Force	91929	1001SD-4-A-1-A	REF
		Pushbutton, Modified	20747	177-015-001	REF

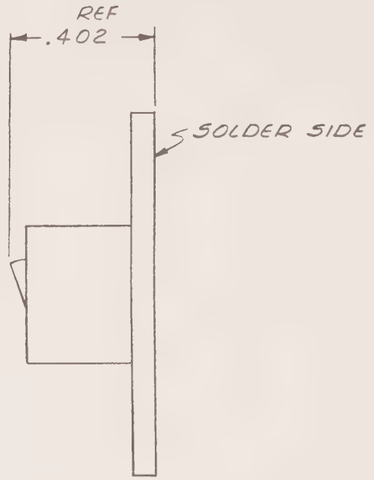
Table 6-8

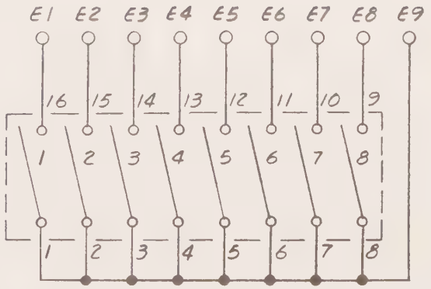
Parts List, FPK001-1 Circuit Card Assy. (cont.)

Reference Designation	Figure No.	Description	Mfg. Code No.	Part No.	Qty.
S24	6-10	Support Switch	91929	1001SD-6-A-1-D	REF
	6-10 (Item 4)	Printed Wiring Board	20747	400-1683	1

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED







NOTES:

1. FOR GENERAL MANUFACTURING & ENGINEERING NOTES SEE DWG. Nº A)401-0010.

QTY	ITEM	FSCM	MONITOR P/N	MFR P/N	DESCRIPTION	NOTES
AR	5	81348	120-101-001	SN63BS	SOLDER	QQ-S-571
	4					
	3					
1	2	00779	107-218-008	435166-5	SWITCH, SPST, 16 PIN	
1	1	20747	400-1611	—	BD, PRINTED WIRING	

501 LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND APPLY BEFORE FINISH
SURFACE ROUGHNESS 125 TOLERANCE ON

FRACTIONS	DECIMALS	ANGLES
± 1/64	± .XX=.02 ± .XXX=.005	± 1° ± 1/2

MATERIAL

FINISH

NEXT ASSY	USED ON
	2003-80

APPLICATION

MONITOR SHOP STANDARDS ARE AN INTEGRAL PART OF THIS DRAWING (298-0077)

800-0187C

Figure 6-11. Unit Code Card Assembly and Parts List

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED PER ECO 05669	10-10-80	D. GREBE
	C	REVISED PER ECO 05928	2-10-81	D. GREBE
	D	REVISED PER ECO 06128	4-7-81	D. GREBE
	E	REVISED PER ECO 06625	9-3-81	D GREBE
	F	REVISED PER ECO 06723	9-3-81	D. GREBE
	G	REVISED PER ECO 07043	12-17-81	M. WALES
	H	REVISED PER ECO 06904	12-30-81	
	J	REVISED PER ECO 07046	1-8-82	
	K	REVISED PER ECO 07138 BANEL 25 JAN 1982	1-27-84	
	L	REVISED PER ECO 08432 FABIC 5-2-83	5-2-83	

GENERAL NOTES

1. For additional information see Assembly Drawing 355-0021-502
2. Unless otherwise indicated, all single wires are MIL-W-16878, type B.
3. Hardware: (lugs, pins, etc.)

*1 (LUG) 118-202-205
*2 (JUMPER) 119-005-027
*3 SYSTEM GROUND LUG
*4 (DIP PLUG) 108-236-002
*5 CINCH 251-22-90-160
*6 (DIP PLUG) 108-236-003
*7 (50 PIN PLUG) 108-236-003
*8 2R5-21051-401 (108-268-003)
*9 (STRAIGHT COAX, 50Ω, PLUG) 108-331-006
*10 (SMA COAX PLUG) 108-333-001
~~*11 (STRAIGHT COAX, 75Ω, PLUG) 108-331-005~~
*12 (BNC, COAX PLUG) 108-303-025
*13 (CONN. 37 PIN) 108-100-008
*14 (DIP PLUG) 131-132-016
*15 (CONN. 25 PIN) 108-100-006
*16 (CONN. 24 PIN) 108-113-008
*17 108-329-008 (50Ω RT ANGLE)
*18 108-329-009 (75Ω RT ANGLE)
*19 790-0650 (CABLE ASSY.)
*20 108-303-001 (CONN. PLUG BNC)
*21 118-213-001 (CONN.-RED SHIELD)

4. ALL CABLES WITH THE DESIGNATION **** MUST BE EQUAL TO ± 0.125 IN. EQUAL LENGTH

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
REVISION	L	H	B	E	F	B	H	H	A	C	H	H	A	H	A	J	K	K	K	H	A	G	G	L

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± | DECIMALS ± | ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
DISTRIBUTION | APPLICATION

CONTRACT NO 2082
DRAWN J. ROMEY 9-4-80 DATE
CHECKED
DRAFTING
ENGINEER J. ROMEY 9-4 80
MFG 9-8-80
APPROVED

AYDIN MONITOR SYSTEMS
FORT WASHINGTON, PENNA. 19034

DATA TRANSMISSION TEST SET, MODEL 607
CHASSIS WIRE LIST

SIZE	CODE IDENT NO		REV.
B	20747	730-1998	L
SCALE —		SHEET 1 OF 24	

800-0982A

Figure 6-12. Model 607 Chassis Wire List (sheet 1)

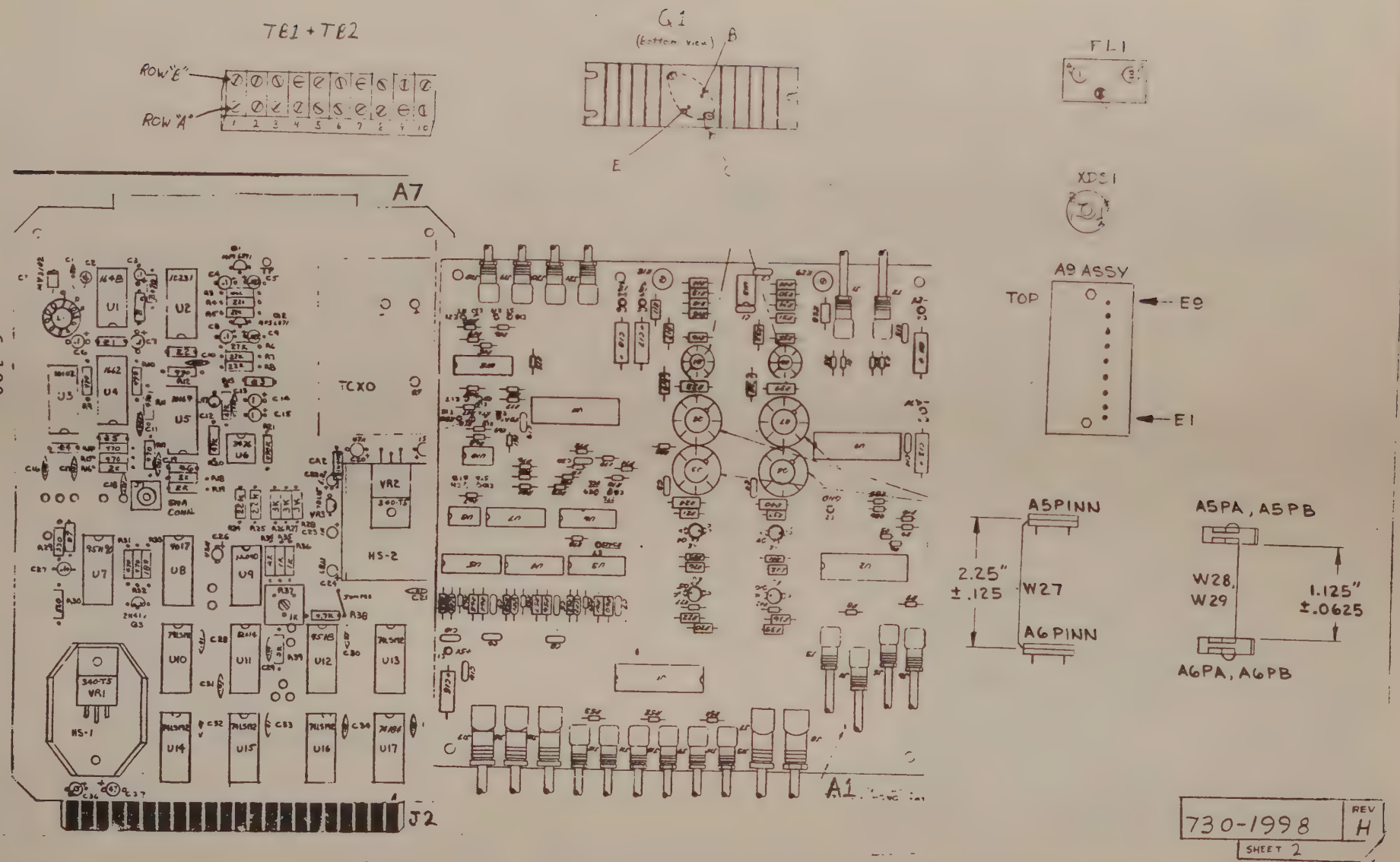
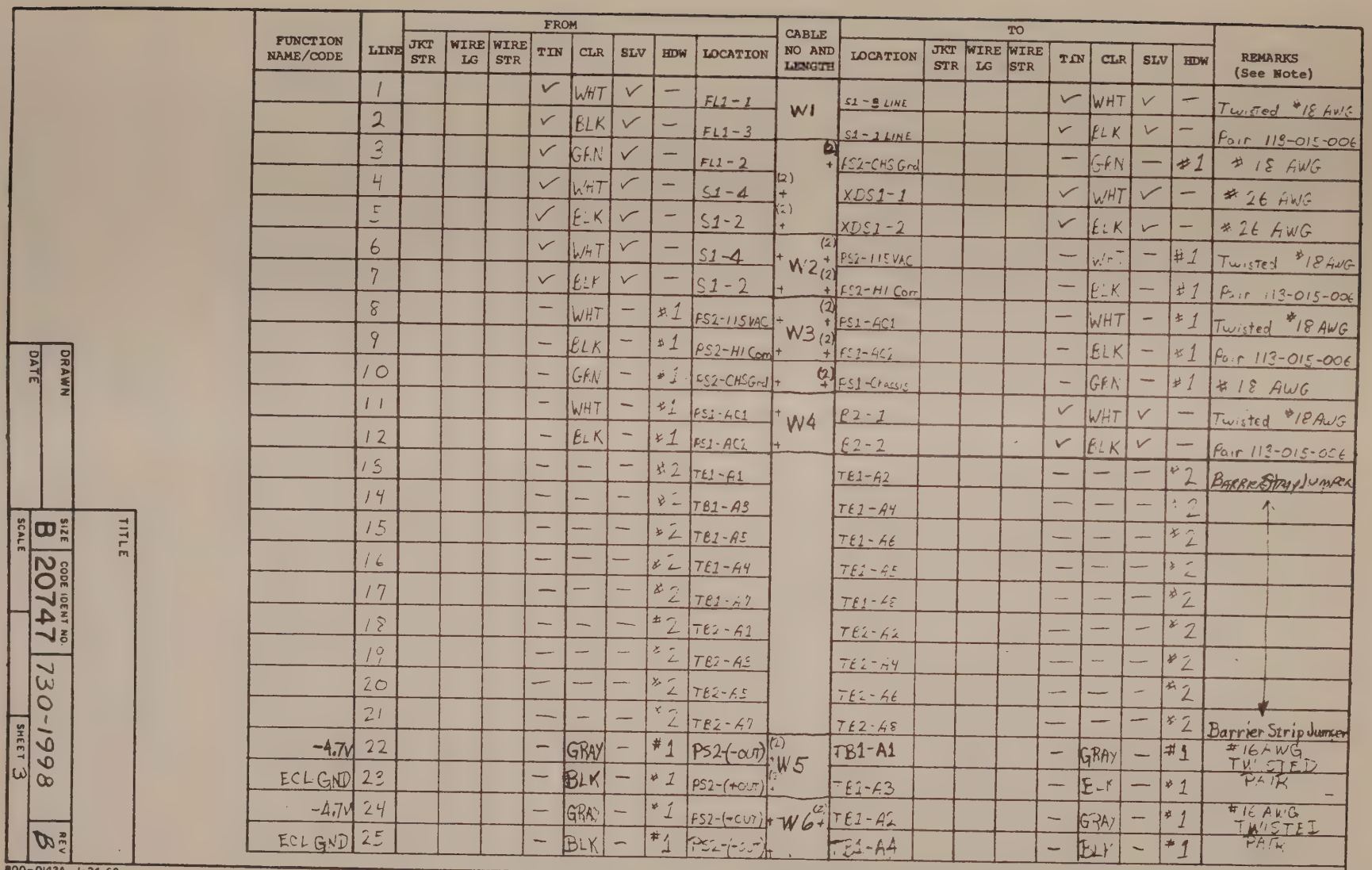


Figure 6-12. Model 607 Chassis Wire List (sheet 2)



FUNCTION NAME/CODE	LINE	FROM: JKT STR	FROM: WIRE LG	FROM: WIRE STR	FROM: TIN	FROM: CLR	FROM: SLV	FROM: HDW	FROM: LOCATION	CABLE NO AND LENGTH	TO: LOCATION	TO: JKT STR	TO: WIRE LG	TO: WIRE STR	TO: TIN	TO: CLR	TO: SLV	TO: HDW	REMARKS (See Note)
	1				✓	WHT	✓	—	FL1-1	W1	S1-S LINE				✓	WHT	✓	—	Twisted #18 AWG
	2				✓	BLK	✓	—	FL1-3		S1-1 LINE				✓	BLK	✓	—	Pair 113-015-006
	3				✓	GRN	✓	—	FL1-2		FS2-CHS Grd				—	GRN	—	#1	#18 AWG
	4				✓	WHT	✓	—	S1-4		XDS1-1				✓	WHT	✓	—	#26 AWG
	5				✓	BLK	✓	—	S1-2		XDS1-2				✓	BLK	✓	—	#26 AWG
	6				✓	WHT	✓	—	S1-4	W2	PS2-115VAC				—	WHT	—	#1	Twisted #18 AWG
	7				✓	BLK	✓	—	S1-2		FS2-HI Com				—	BLK	—	#1	Pair 113-015-006
	8				—	WHT	—	#1	PS2-115VAC	W3	PS1-AC1				—	WHT	—	#1	Twisted #18 AWG
	9				—	BLK	—	#1	PS2-HI Com		PS1-AC2				—	BLK	—	#1	Pair 113-015-006
	10				—	GRN	—	#1	CS2-CHSGrd		FS1-Chassis				—	GRN	—	#1	#18 AWG
	11				—	WHT	—	#1	PS1-AC1	W4	E2-1				✓	WHT	✓	—	Twisted #18 AWG
	12				—	BLK	—	#1	PS1-AC2		E2-2				✓	BLK	✓	—	Pair 113-015-006
	13				—	—	—	#2	TE1-A1		TE1-A2				—	—	—	#2	Barrier Strip Jumper
	14				—	—	—	#2	TB1-A3		TE1-A4				—	—	—	#2	↑
	15				—	—	—	#2	TB1-A5		TE1-A6				—	—	—	#2	
	16				—	—	—	#2	TE1-A4		TE1-A5				—	—	—	#2	
	17				—	—	—	#2	TE1-A7		TE1-A8				—	—	—	#2	
	18				—	—	—	#2	TE2-A1		TE2-A2				—	—	—	#2	
	19				—	—	—	#2	TE2-A3		TE2-A4				—	—	—	#2	
	20				—	—	—	#2	TE2-A5		TE2-A6				—	—	—	#2	
	21				—	—	—	#2	TE2-A7		TE2-A8				—	—	—	#2	Barrier Strip Jumper
-4.7V	22				—	GRAY	—	#1	PS2-(-OUT)	W5	TB1-A1				—	GRAY	—	#1	#16 AWG TWISTED PAIR
ECL GND	23				—	BLK	—	#1	PS2-(+OUT)		TE1-A3				—	BLK	—	#1	
-4.7V	24				—	GRAY	—	#1	PS2-(+OUT)	W6	TE1-A2				—	GRAY	—	#1	#16 AWG TWISTED PAIR
ECL GND	25				—	BLK	—	#1	PS2-(-OUT)		TE1-A4				—	BLK	—	#1	

DRAWN
DATE
SIZE B
CODE IDENT NO. 20747
SCALE
SHEET 3
REV B
TITLE
730-1998
800-0142A, 1-24-68

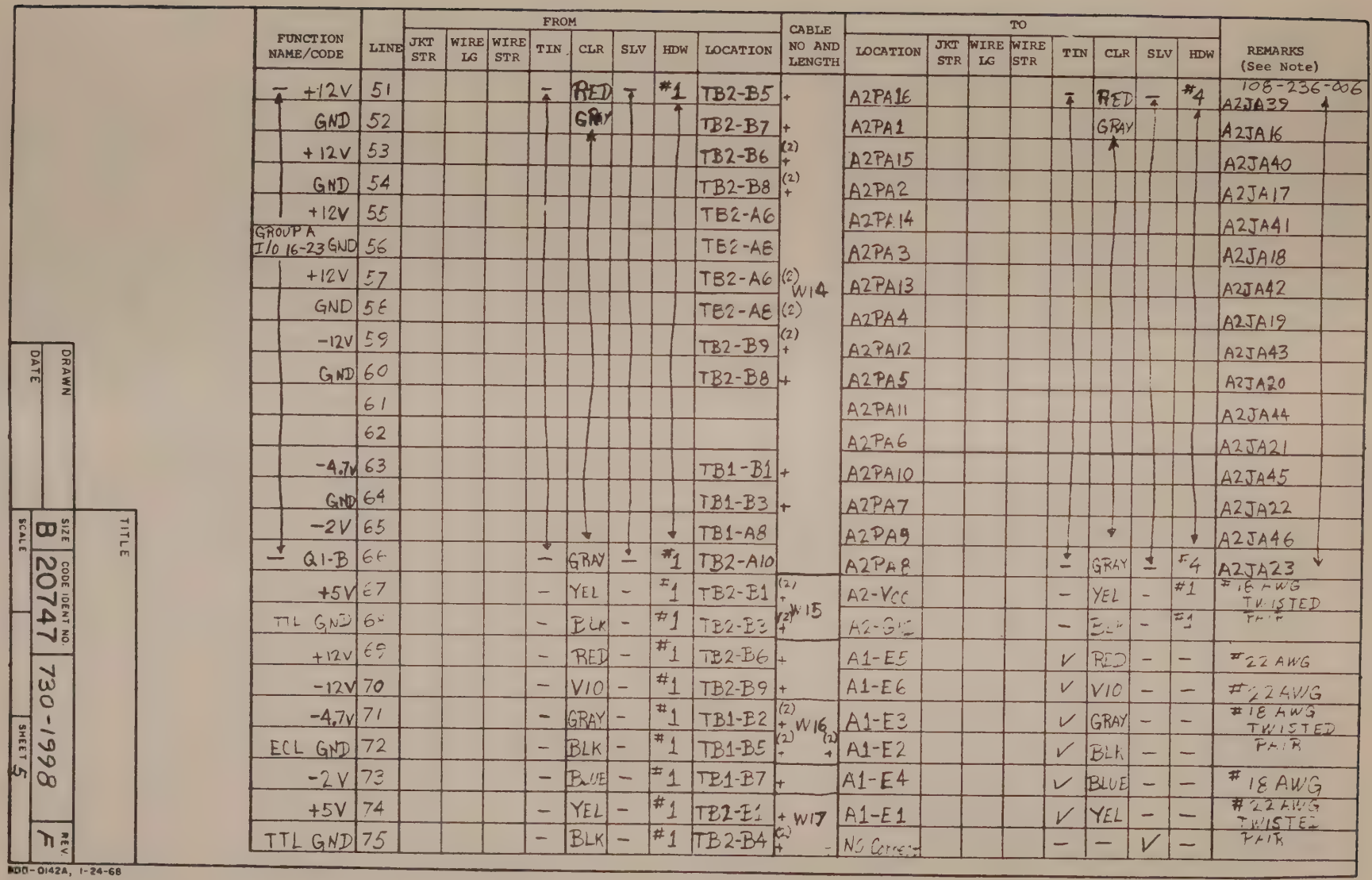
Figure 6-12. Model 607 Chassis Wire List (sheet 3)

FUNCTION NAME/CODE	LINE	FROM								CABLE NO AND LENGTH	TO								REMARKS (See Note)
		JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION		LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	
+5V	26				–	YEL	–	#1	PS1-(+A1)	(1) W7 (2)	TE2-A1				–	YEL	–	#1	Twisted #18 AWG
TTL GND	27				–	BLK	–	#1	PS1-Com 2		TE2-A3				–	BLK	–	#1	Pair
+12V	28				–	RED	–	#1	PS1-(+E)		TE2-A5				–	RED	–	#1	Twisted #18 AWG
-12V	29				–	VIO	–	#1	PS1-(-C)	W8	TE2-A9				–	VIO	–	#1	
±12V GND	30				–	BLK	–	#1	PS1-Com 1		TE2-A7				–	BLK	–	#1	Twisted
	31				–	GRN	–	#1	TE1-E1	(2) W9	G1-C				✓	GRN	–	–	Twisted #18 AWG
	32				–	BLK	–	#1	TE1-E3	(2)	NO CONNECTION				–	BLK		–	Pair
	33				–	BLUE	–	#1	TE1-E7	(2) W10	G1-E				✓	BLUE	–	–	Twisted #16 AWG
	34				–	BLK	–	#1	TE1-E4		NO CONNECTION				–	BLK	–	–	Pair
	35				–	GRN	–	#1	PS1-Chassis	(2)	TB1-B10				–	GRN	–	#1	
	36				–	–	–	–	TE1-A9		R1-1				–	–	–	#1	INSTALL INSULATING TUBING
	37				–	–	–	–	TE1-A10		R1-2				–	–	–	#1	
	38				–	BLK	–	#1	TE2-A4	(2)	TE1-E5				–	BLK	–	#1	#18AWG
TTL to ECL GND	39				–	BLK	–	#1	TE2-A3	(2)	TB1-A6				–	BLK	–	#1	#16AWG
SIG GND	40				–	BLK	–	#1	TB1-A6		FLAT PART E2				–	BLK	–	#3	#16AWG SHIELD GND
	41																		
+12V	42				–	RED	–	#1	TE2-E5	(2) W11 (2)	A7J2-Y				✓	RED	✓	#5	#18 AWG TWISTED
GND	43				–	BLK	–	#1	TE2-E7	(2)	A7J2-Z				✓	BLK	✓	#5	PAIR
+12V	44				✓	RED	✓	#5	A7J2-1		A7J2-Y				✓	RED	✓	#5	#22 AWG
	45																		
	46				–	GRN	–	#1	TB2-B10	W12	Q1-B				✓	GRN	✓	–	#26 AWG TWISTED
	47				–	BLK	–	#1	TB2-A8		No Connect				–	BLK	✓	–	PAIR
+5V	48				–	YEL	–	#1	PS1-(+A1)	W13	TB2-A2				–	YEL	–	#1	#16 AWG TWISTED
TTL GND	49				–	BLK	–	#1	PS1-Com 2		TB2-A4				–	BLK	–	#1	PAIR
	50																		

DRAWN
DATE
TITLE
SIZE B
CODE IDENT NO. 20747
SCALE
SHEET 4
730-1998
REV E

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 4)

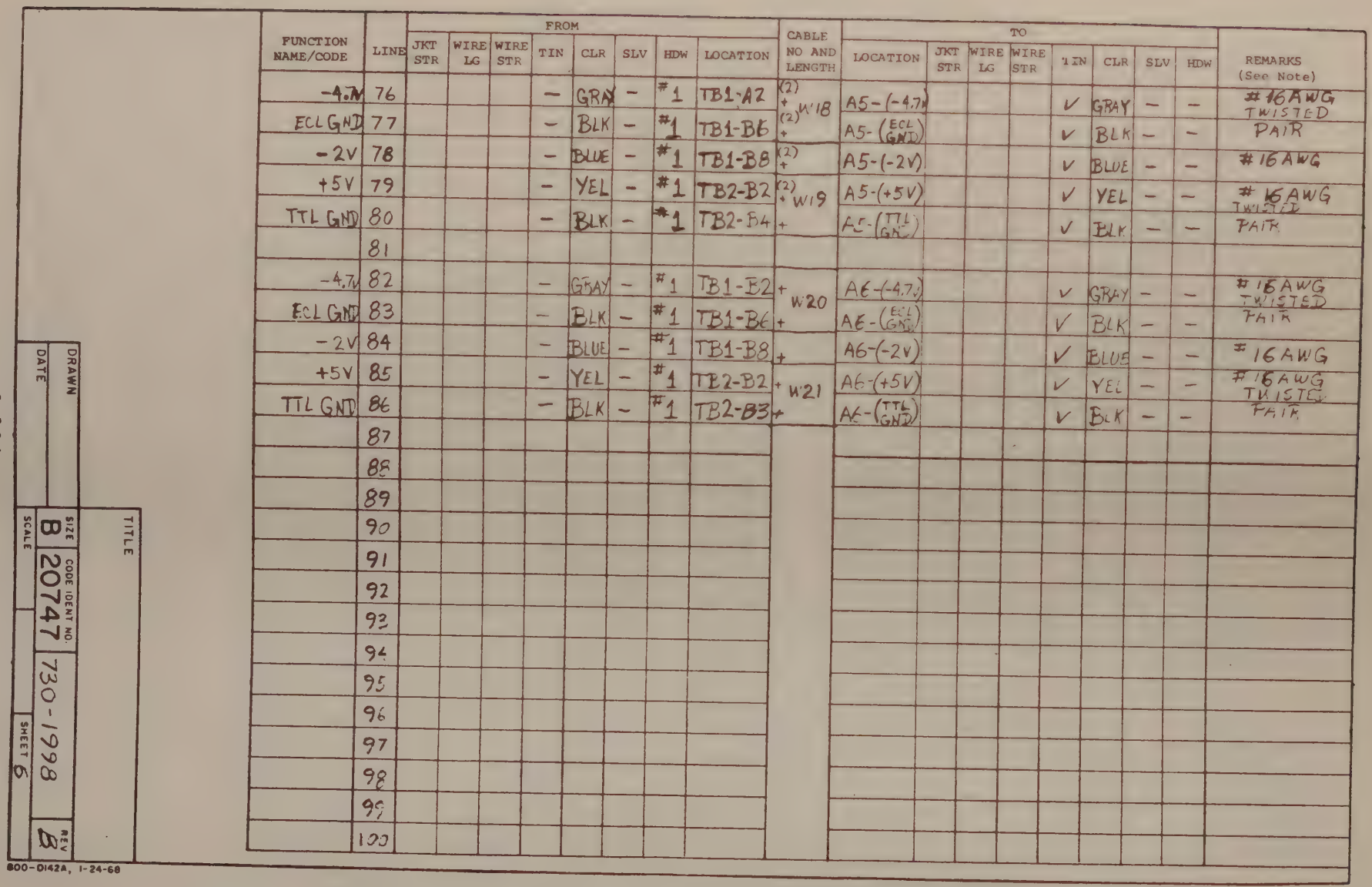


FUNCTION NAME/CODE	LINE	FROM: JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION	CABLE NO AND LENGTH	TO: LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	REMARKS (See Note)
+12V	51				–	RED	–	#1	TB2-B5	+	A2PA16				–	RED	–	#4	108-236-006 A2JA39
GND	52					GRAY			TB2-B7	+	A2PA1					GRAY			A2JA16
+12V	53								TB2-B6	(2) +	A2PA15								A2JA40
GND	54								TB2-B8	(2) +	A2PA2								A2JA17
+12V	55								TB2-A6		A2PA14								A2JA41
GROUP A I/O 16-23 GND	56								TB2-A8		A2PA3								A2JA18
+12V	57								TB2-A6	(2) W14	A2PA13								A2JA42
GND	58								TB2-A8	(2)	A2PA4								A2JA19
-12V	59								TB2-B9	(2) +	A2PA12								A2JA43
GND	60								TB2-B8	+	A2PA5								A2JA20
	61										A2PA11								A2JA44
	62										A2PA6								A2JA21
-4.7V	63								TB1-B1	+	A2PA10								A2JA45
GND	64								TB1-B3	+	A2PA7								A2JA22
-2V	65								TB1-A8		A2PA9								A2JA46
Q1-B	66				–	GRAY	–	#1	TB2-A10		A2PA8				–	GRAY	–	#4	A2JA23
+5V	67				–	YEL	–	#1	TB2-B1	(2) + W15	A2-Vcc				–	YEL	–	#1	#18 AWG TWISTED PAIR
TTL GND	68				–	BLK	–	#1	TB2-B3	(2) +	A2-GND				–	BLK	–	#1	
+12V	69				–	RED	–	#1	TB2-B6	+	A1-E5				V	RED	–	–	#22 AWG
-12V	70				–	VIO	–	#1	TB2-B9	+	A1-E6				V	VIO	–	–	#22 AWG
-4.7V	71				–	GRAY	–	#1	TB1-B2	(2) + W16	A1-E3				V	GRAY	–	–	#18 AWG TWISTED PAIR
ECL GND	72				–	BLK	–	#1	TB1-B5	(2) + (2) +	A1-E2				V	BLK	–	–	
-2V	73				–	BLUE	–	#1	TB1-B7	+	A1-E4				V	BLUE	–	–	#18 AWG
+5V	74				–	YEL	–	#1	TB2-E1	+ W17	A1-E1				V	YEL	–	–	#22 AWG TWISTED PAIR
TTL GND	75				–	BLK	–	#1	TB2-B4	(2) +	NO CONNECT				–	–	V	–	

DRAWN
DATE
SIZE B
CODE IDENT NO 20747
SCALE
SHEET 5
REV F
TITLE 730-1998

BDD-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 5)

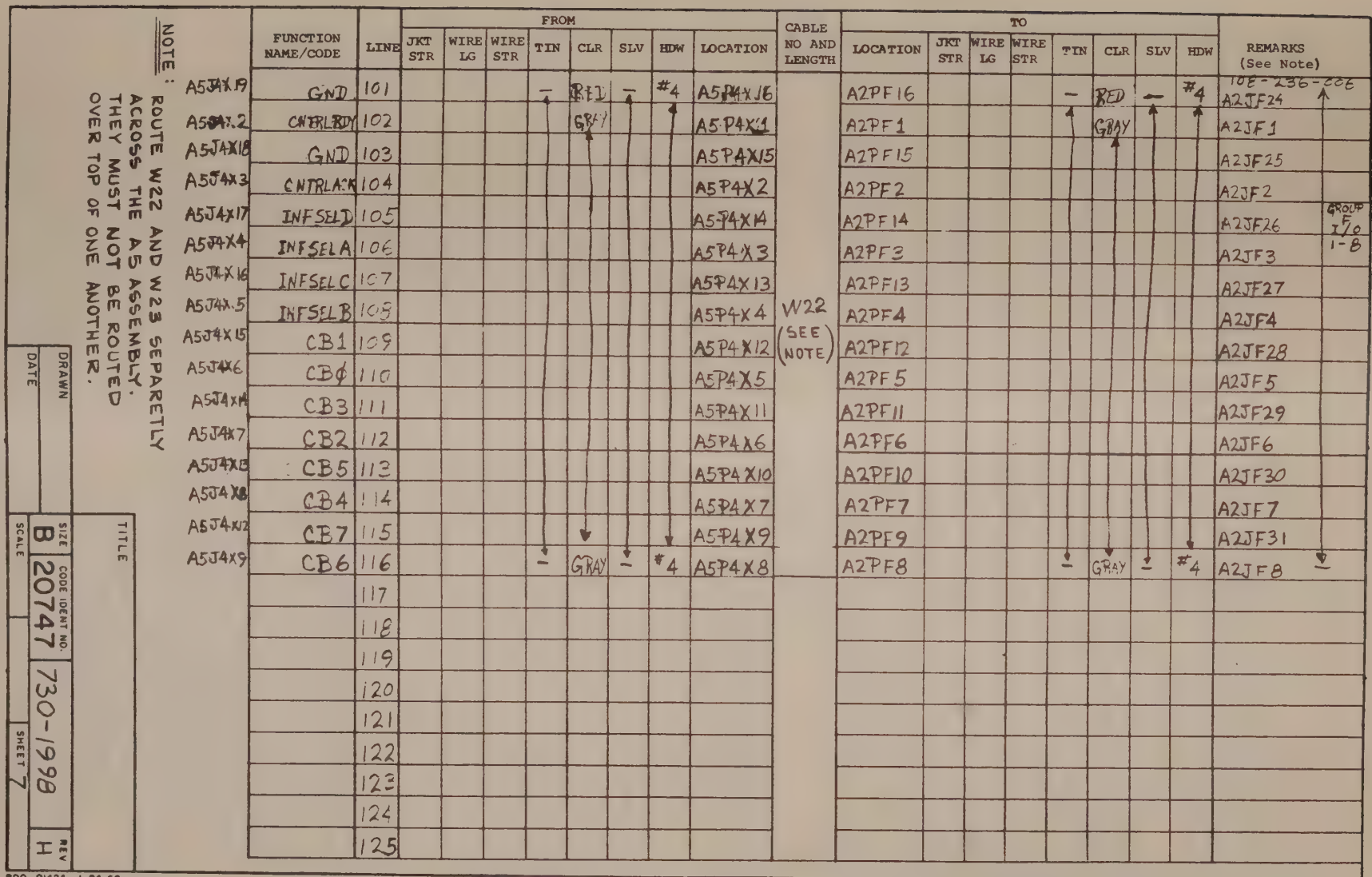


FUNCTION NAME/CODE	LINE	FROM: JKT STR	FROM: WIRE LG	FROM: WIRE STR	FROM: TIN	FROM: CLR	FROM: SLV	FROM: HDW	FROM: LOCATION	CABLE NO AND LENGTH	TO: LOCATION	TO: JKT STR	TO: WIRE LG	TO: WIRE STR	TO: TIN	TO: CLR	TO: SLV	TO: HDW	REMARKS (See Note)
-4.7V	76				–	GRAY	–	#1	TB1-A2	(2) + (2) W18 +	A5-(-4.7V)				✓	GRAY	–	–	#16AWG TWISTED
ECL GND	77				–	BLK	–	#1	TB1-B6		A5-(ECL GND)				✓	BLK	–	–	PAIR
-2V	78				–	BLUE	–	#1	TB1-B8	(2) +	A5-(-2V)				✓	BLUE	–	–	#16AWG
+5V	79				–	YEL	–	#1	TB2-B2	(2) + W19	A5-(+5V)				✓	YEL	–	–	#16AWG TWISTED
TTL GND	80				–	BLK	–	#1	TB2-B4	+	A5-(TTL GND)				✓	BLK	–	–	PAIR
	81																		
-4.7V	82				–	GRAY	–	#1	TB1-B2	+ W20	A6-(-4.7V)				✓	GRAY	–	–	#16AWG TWISTED
ECL GND	83				–	BLK	–	#1	TB1-B6	+	A6-(ECL GND)				✓	BLK	–	–	PAIR
-2V	84				–	BLUE	–	#1	TB1-B8	+	A6-(-2V)				✓	BLUE	–	–	#16AWG
+5V	85				–	YEL	–	#1	TB2-B2	+ W21	A6-(+5V)				✓	YEL	–	–	#16AWG TWISTED
TTL GND	86				–	BLK	–	#1	TB2-B3	+	A6-(TTL GND)				✓	BLK	–	–	PAIR
	87																		
	88																		
	89																		
	90																		
	91																		
	92																		
	93																		
	94																		
	95																		
	96																		
	97																		
	98																		
	99																		
	100																		

DRAWN
DATE
TITLE
SIZE B
CODE IDENT NO. 20747
730-1998
SCALE
SHEET 6
REV B

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 6)



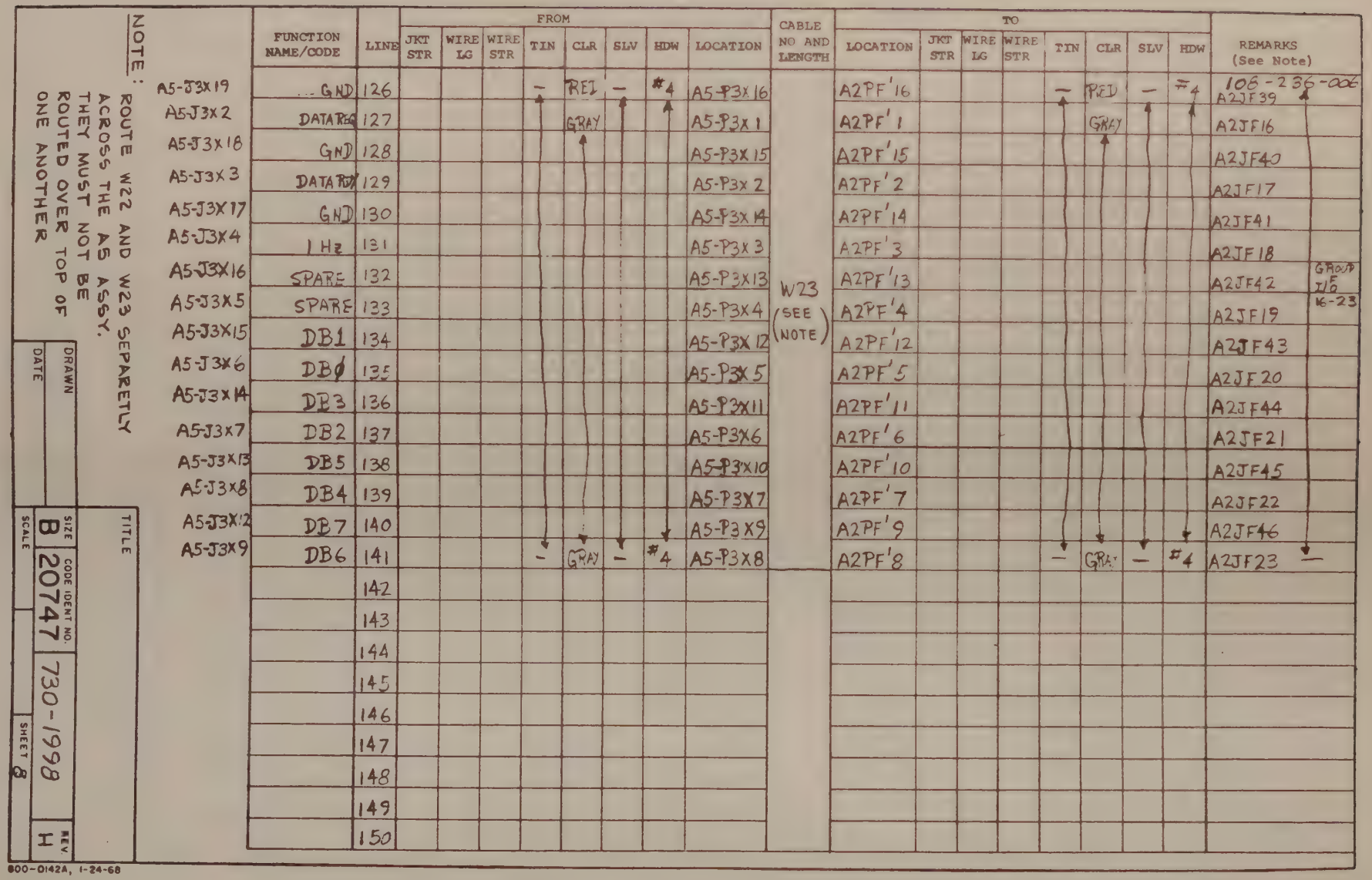
NOTE: ROUTE W22 AND W23 SEPARETLY ACROSS THE A5 ASSEMBLY. THEY MUST NOT BE ROUTED OVER TOP OF ONE ANOTHER.

	FUNCTION NAME/CODE	LINE	FROM: JKT STR	FROM: WIRE LG	FROM: WIRE STR	FROM: TIN	FROM: CLR	FROM: SLV	FROM: HDW	FROM: LOCATION	CABLE NO AND LENGTH	TO: LOCATION	TO: JKT STR	TO: WIRE LG	TO: WIRE STR	TO: TIN	TO: CLR	TO: SLV	TO: HDW	REMARKS (See Note)
A5J4X19	GND	101				—	RED	—	#4	A5P4X16		A2PF16				—	RED	—	#4	10E-236-20E A2JF24
A5J4X2	CNTRLBDY	102					GRAY			A5P4X1		A2PF1					GRAY			A2JF1
A5J4X18	GND	103								A5P4X15		A2PF15								A2JF25
A5J4X3	CNTRLACK	104								A5P4X2		A2PF2								A2JF2
A5J4X17	INFSELD	105								A5P4X14		A2PF14								A2JF26 GROUP I/O I-B
A5J4X4	INFSELA	106								A5P4X3		A2PF3								A2JF3
A5J4X16	INFSELC	107								A5P4X13		A2PF13								A2JF27
A5J4X5	INFSELB	108								A5P4X4	W22 (SEE NOTE)	A2PF4								A2JF4
A5J4X15	CB1	109								A5P4X12		A2PF12								A2JF28
A5J4X6	CB0	110								A5P4X5		A2PF5								A2JF5
A5J4X14	CB3	111								A5P4X11		A2PF11								A2JF29
A5J4X7	CB2	112								A5P4X6		A2PF6								A2JF6
A5J4X13	CB5	113								A5P4X10		A2PF10								A2JF30
A5J4X8	CB4	114								A5P4X7		A2PF7								A2JF7
A5J4X12	CB7	115								A5P4X9		A2PF9								A2JF31
A5J4X9	CB6	116				—	GRAY	—	#4	A5P4X8		A2PF8				—	GRAY	—	#4	A2JF8
		117																		
		118																		
		119																		
		120																		
		121																		
		122																		
		123																		
		124																		
		125																		

DRAWN
DATE
SIZE B
CODE IDENT NO. 20747
SHEET 7
REV H
SCALE
TITLE
730-1998

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 7)



NOTE: ROUTE W22 AND W23 SEPARETLY ACROSS THE A5 ASSY. THEY MUST NOT BE ROUTED OVER TOP OF ONE ANOTHER

FUNCTION NAME/CODE	LINE	FROM: JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION	CABLE NO AND LENGTH	TO: LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	REMARKS (See Note)
A5-J3X19 GND	126				–	RED	–	#4	A5-P3X16	W23 (SEE NOTE)	A2PF'16				–	RED	–	#4	106-236-006 A2JF39
A5-J3X2 DATA RET	127					GRAY			A5-P3X1		A2PF'1					GRAY			A2JF16
A5-J3X18 GND	128								A5-P3X15		A2PF'15								A2JF40
A5-J3X3 DATA RDY	129								A5-P3X2		A2PF'2								A2JF17
A5-J3X17 GND	130								A5-P3X14		A2PF'14								A2JF41
A5-J3X4 1 Hz	131								A5-P3X3		A2PF'3								A2JF18
A5-J3X16 SPARE	132								A5-P3X13		A2PF'13								A2JF42 GROUP J6 K-23
A5-J3X5 SPARE	133								A5-P3X4		A2PF'4								A2JF19
A5-J3X15 DB1	134								A5-P3X12		A2PF'12								A2JF43
A5-J3X6 DB0	135								A5-P3X5		A2PF'5								A2JF20
A5-J3X14 DB3	136								A5-P3X11		A2PF'11								A2JF44
A5-J3X7 DB2	137								A5-P3X6		A2PF'6								A2JF21
A5-J3X13 DB5	138								A5-P3X10		A2PF'10								A2JF45
A5-J3X8 DB4	139								A5-P3X7		A2PF'7								A2JF22
A5-J3X12 DB7	140								A5-P3X9		A2PF'9								A2JF46
A5-J3X9 DB6	141				–	GRAY	–	#4	A5-P3X8		A2PF'8				–	GRAY	–	#4	A2JF23 –
	142																		
	143																		
	144																		
	145																		
	146																		
	147																		
	148																		
	149																		
	150																		

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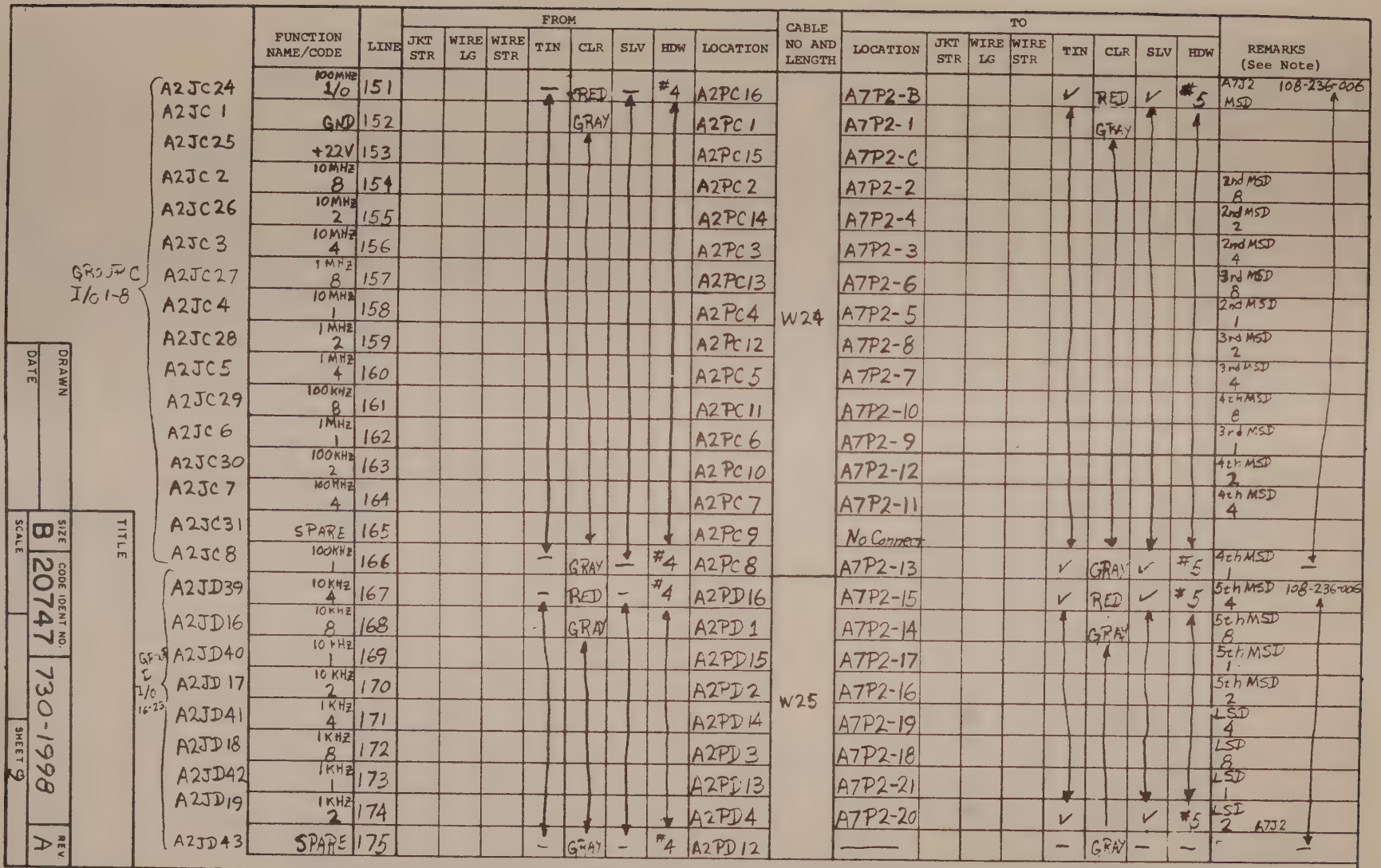
Fiugre 6-12. Model 607 Chassis Wire List (sheet 8)



FUNCTION NAME/CODE	LINE	FROM: JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION	CABLE NO AND LENGTH	TO: LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	REMARKS (See Note)
A2JC24 100MHz 1/0	151				—	RED	—	#4	A2PC16		A7P2-B				✓	RED	✓	#5	A7J2 108-236-006 MSD
A2JC1 GND	152					GRAY			A2PC1		A7P2-1					GRAY			
A2JC25 +22V	153								A2PC15		A7P2-C								
A2JC2 10MHz 8	154								A2PC2		A7P2-2								2nd MSD 8
A2JC26 10MHz 2	155								A2PC14		A7P2-4								2nd MSD 2
A2JC3 10MHz 4	156								A2PC3		A7P2-3								2nd MSD 4
A2JC27 1MHz 8	157								A2PC13		A7P2-6								3rd MSD 8
A2JC4 10MHz 1	158								A2PC4	W24	A7P2-5								2nd MSD 1
A2JC28 1MHz 2	159								A2PC12		A7P2-8								3rd MSD 2
A2JC5 1MHz 4	160								A2PC5		A7P2-7								3rd MSD 4
A2JC29 100KHz 8	161								A2PC11		A7P2-10								4th MSD 8
A2JC6 1MHz 1	162								A2PC6		A7P2-9								3rd MSD 1
A2JC30 100KHz 2	163								A2PC10		A7P2-12								4th MSD 2
A2JC7 10MHz 4	164								A2PC7		A7P2-11								4th MSD 4
A2JC31 SPARE	165								A2PC9		No Connect								
A2JC8 100KHz 1	166				—	GRAY	—	#4	A2PC8		A7P2-13				✓	GRAY	✓	#5	4th MSD 1 —
A2JD39 10KHz 4	167				—	RED	—	#4	A2PD16		A7P2-15				✓	RED	✓	#5	5th MSD 4 108-236-006
A2JD16 10KHz 8	168					GRAY			A2PD1		A7P2-14					GRAY			5th MSD 8
A2JD40 10KHz 1	169								A2PD15		A7P2-17								5th MSD 1
A2JD17 10KHz 2	170								A2PD2		A7P2-16								5th MSD 2
A2JD41 1KHz 4	171								A2PD14	W25	A7P2-19								LSD 4
A2JD18 1KHz 8	172								A2PD3		A7P2-18								LSD 8
A2JD42 1KHz 1	173								A2PD13		A7P2-21								LSD 1
A2JD19 1KHz 2	174								A2PD4		A7P2-20				✓		✓	#5	LSD 2 A7J2
A2JD43 SPARE	175				—	GRAY	—	#4	A2PD12		———				—	GRAY	—	—	— —

GROUP C I/O 1-8

GROUP C I/O 16-23

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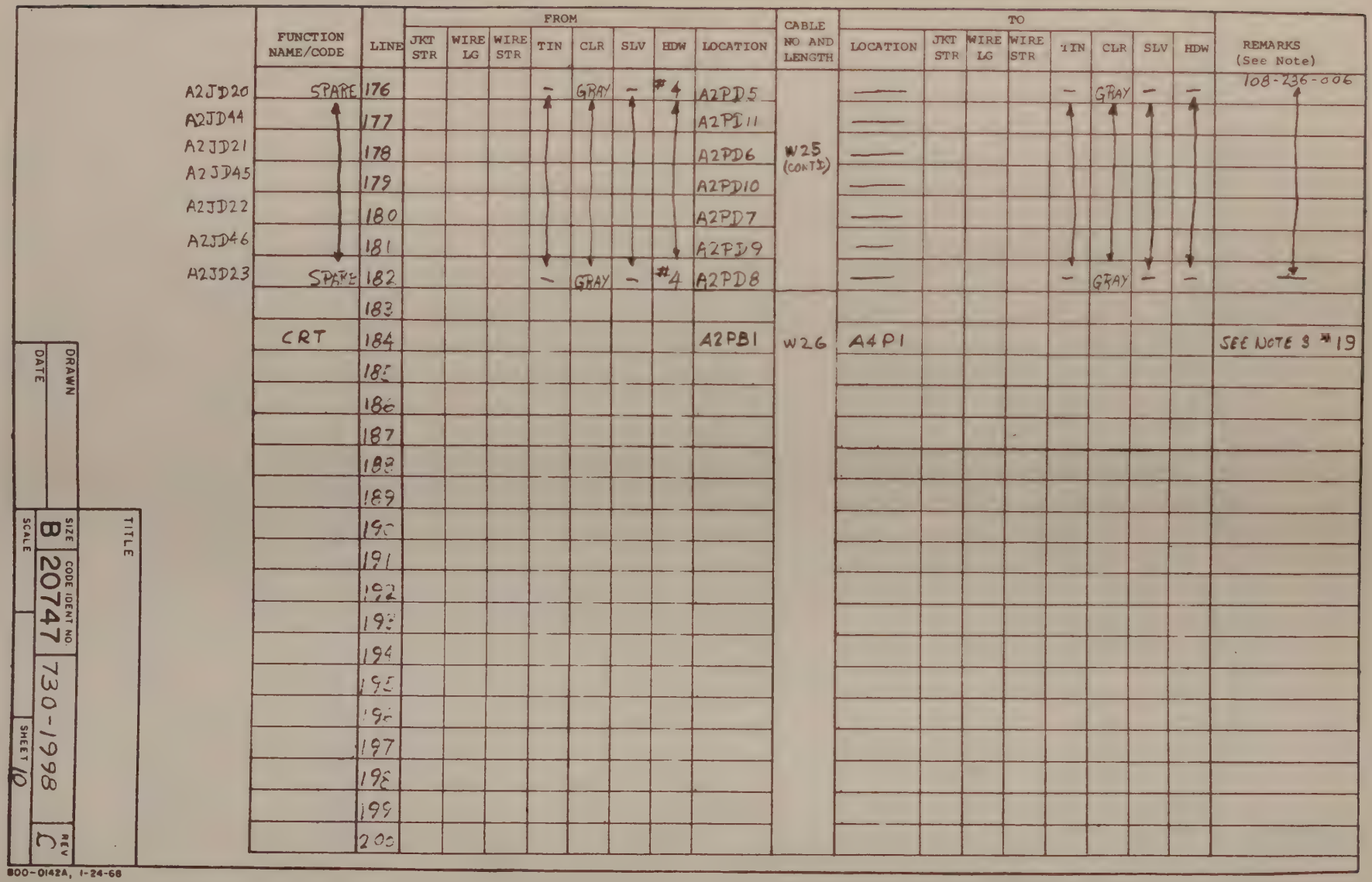
Figure 6-12. Model 607 Chassis Wire List (sheet 9)



	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A2JD20	SPARE	176				–	GRAY	–	#4	A2PD5		—				–	GRAY	–	–	108-236-006
A2JD44		177								A2PD11		—								
A2JD21		178								A2PD6	W25 (CONT'D)	—								
A2JD45		179								A2PD10		—								
A2JD22		180								A2PD7		—								
A2JD46		181								A2PD9		—								
A2JD23	SPARE	182				–	GRAY	–	#4	A2PD8		—				–	GRAY	–	–	
		183																		
	CRT	184								A2PB1	W26	A4P1								SEE NOTE 3 #19
		185																		
		186																		
		187																		
		188																		
		189																		
		190																		
		191																		
		192																		
		193																		
		194																		
		195																		
		196																		
		197																		
		198																		
		199																		
		200																		

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Figure 6-12. Model 607 Chassis Wire List (sheet 10)

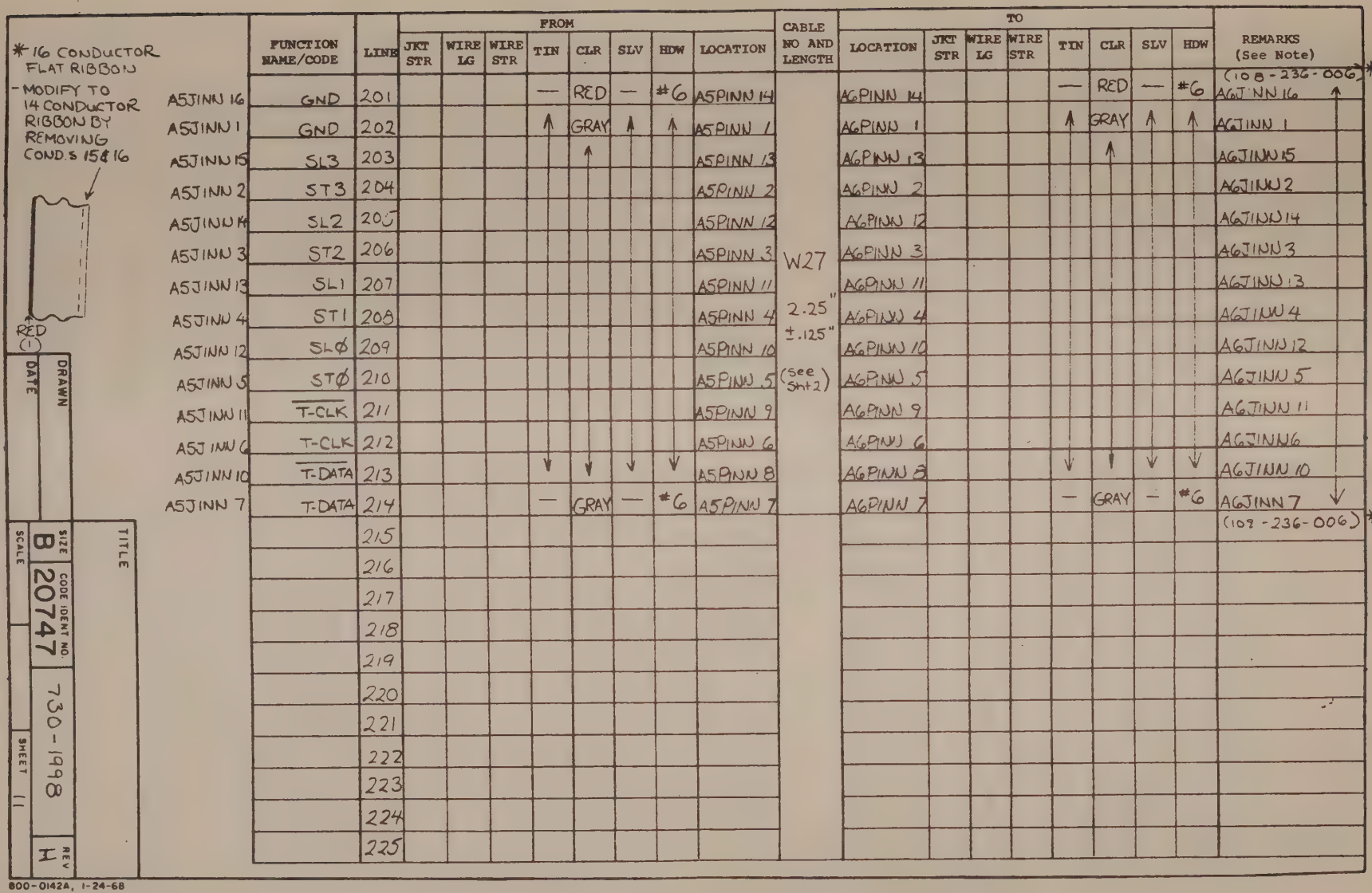
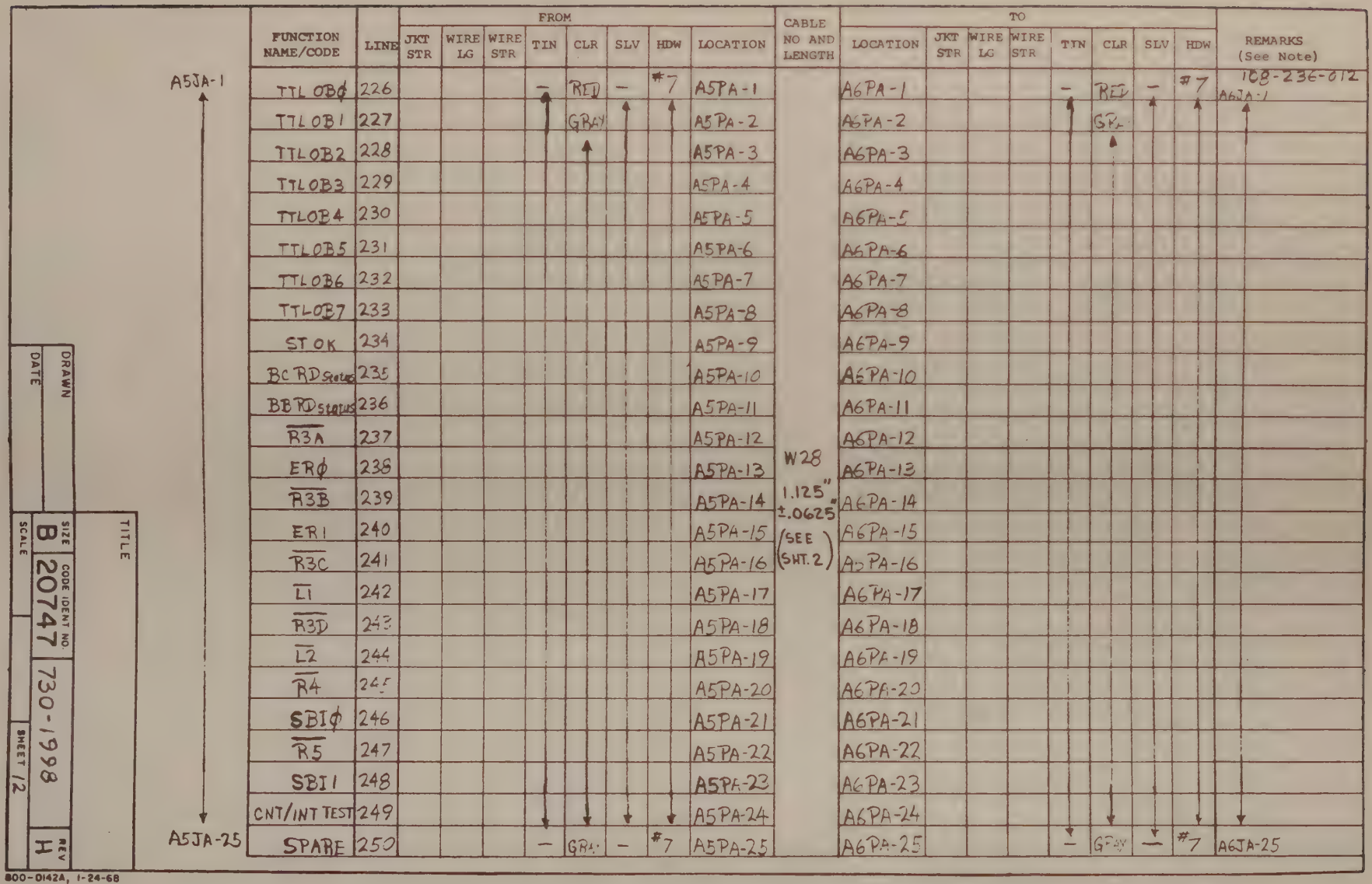


Figure 6-12. Model 607 Chassis Wire List (sheet 11)



	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A5JA-1	TTL OBϕ	226				–	RED	–	#7	A5PA-1		A6PA-1				–	RED	–	#7	108-236-012 A6JA-1
	TTLOB1	227					GRAY			A5PA-2		A6PA-2					GR.			
	TTLOB2	228								A5PA-3		A6PA-3								
	TTLOB3	229								A5PA-4		A6PA-4								
	TTLOB4	230								A5PA-5		A6PA-5								
	TTLOB5	231								A5PA-6		A6PA-6								
	TTLOB6	232								A5PA-7		A6PA-7								
	TTLOB7	233								A5PA-8		A6PA-8								
	STOK	234								A5PA-9		A6PA-9								
	BCRD status	235								A5PA-10		A6PA-10								
	BBRD status	236								A5PA-11		A6PA-11								
	$\overline{R3A}$	237								A5PA-12		A6PA-12								
	ERϕ	238								A5PA-13	W28 1.125" ±.0625 (SEE SHT. 2)	A6PA-13								
	$\overline{R3B}$	239								A5PA-14		A6PA-14								
	ER1	240								A5PA-15		A6PA-15								
	$\overline{R3C}$	241								A5PA-16		A6PA-16								
	$\overline{L1}$	242								A5PA-17		A6PA-17								
	$\overline{R3D}$	243								A5PA-18		A6PA-18								
	$\overline{L2}$	244								A5PA-19		A6PA-19								
	$\overline{R4}$	245								A5PA-20		A6PA-20								
	SBIϕ	246								A5PA-21		A6PA-21								
	$\overline{R5}$	247								A5PA-22		A6PA-22								
	SBI1	248								A5PA-23		A6PA-23								
	CNT/INT TEST	249								A5PA-24		A6PA-24								
A5JA-25	SPARE	250				–	GRAY	–	#7	A5PA-25		A6PA-25				–	GRAY	–	#7	A6JA-25

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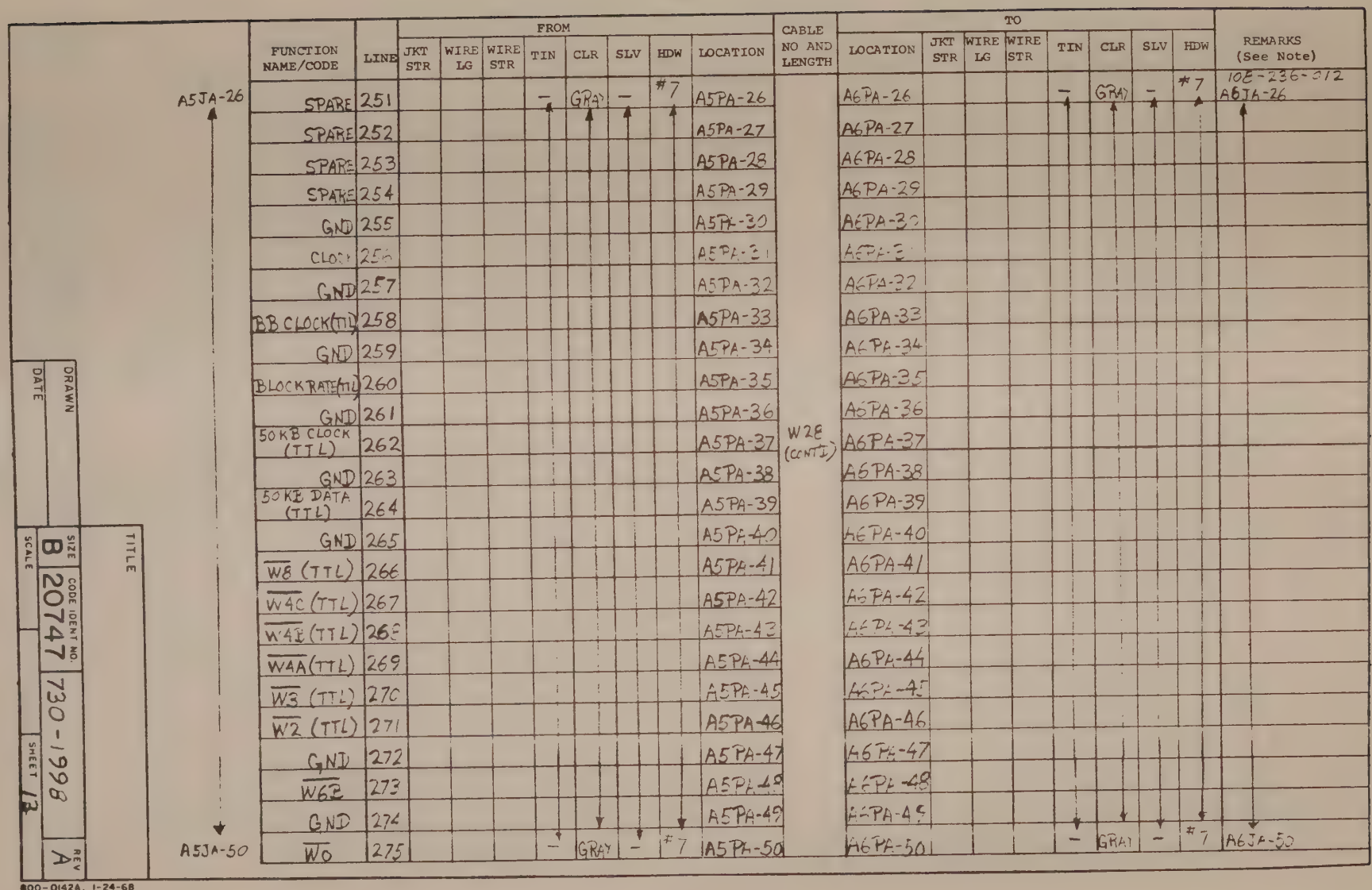
Figure 6-12. Model 607 Chassis Wire List (sheet 12)



	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A5JA-26	SPARE	251				–	GRAY	–	#7	A5PA-26		A6PA-26				–	GRAY	–	#7	10E-236-012 A6JA-26
	SPARE	252								A5PA-27		A6PA-27								
	SPARE	253								A5PA-28		A6PA-28								
	SPARE	254								A5PA-29		A6PA-29								
	GND	255								A5PA-30		A6PA-30								
	CLOCK	256								A5PA-31		A6PA-31								
	GND	257								A5PA-32		A6PA-32								
	BB CLOCK(TTL)	258								A5PA-33		A6PA-33								
	GND	259								A5PA-34		A6PA-34								
	BLOCK RATE(TTL)	260								A5PA-35		A6PA-35								
	GND	261								A5PA-36		A6PA-36								
	50KB CLOCK (TTL)	262								A5PA-37	W2E (CONT'D)	A6PA-37								
	GND	263								A5PA-38		A6PA-38								
	50KB DATA (TTL)	264								A5PA-39		A6PA-39								
	GND	265								A5PA-40		A6PA-40								
	$\overline{W8}$ (TTL)	266								A5PA-41		A6PA-41								
	$\overline{W4C}$ (TTL)	267								A5PA-42		A6PA-42								
	$\overline{W4B}$ (TTL)	268								A5PA-43		A6PA-43								
	$\overline{W4A}$ (TTL)	269								A5PA-44		A6PA-44								
	$\overline{W3}$ (TTL)	270								A5PA-45		A6PA-45								
	$\overline{W2}$ (TTL)	271								A5PA-46		A6PA-46								
	GND	272								A5PA-47		A6PA-47								
	$\overline{W6B}$	273								A5PA-48		A6PA-48								
	GND	274								A5PA-49		A6PA-49								
A5JA-50	$\overline{W0}$	275				–	GRAY	–	#7	A5PA-50		A6PA-50				–	GRAY	–	#7	A6JA-50

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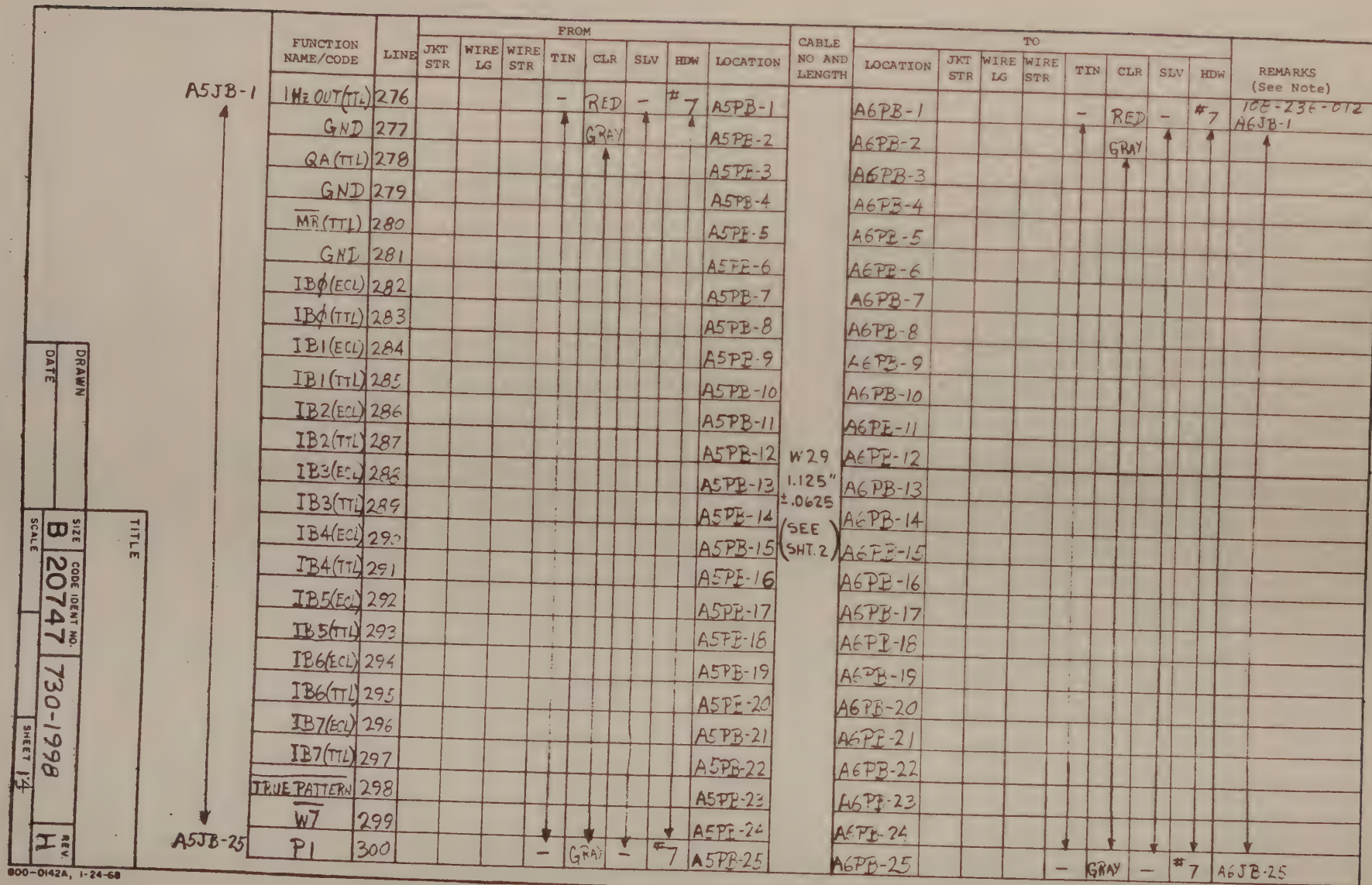
Figure 6-12. Model 607 Chassis Wire List (sheet 13)



FUNCTION NAME/CODE	LINE	FROM: JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION	CABLE NO AND LENGTH	TO: LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	REMARKS (See Note)
A5JB-1																			
1MHz OUT(TTL)	276				-	RED	-	#7	A5PB-1		A6PB-1				-	RED	-	#7	10E-236-012 A6JB-1
GND	277					GRAY			A5PB-2		A6PB-2					GRAY			
QA(TTL)	278								A5PB-3		A6PB-3								
GND	279								A5PB-4		A6PB-4								
$\overline{MR}$(TTL)	280								A5PB-5		A6PB-5								
GND	281								A5PB-6		A6PB-6								
IBØ(ECL)	282								A5PB-7		A6PB-7								
IBØ(TTL)	283								A5PB-8		A6PB-8								
IB1(ECL)	284								A5PB-9		A6PB-9								
IB1(TTL)	285								A5PB-10		A6PB-10								
IB2(ECL)	286								A5PB-11		A6PB-11								
IB2(TTL)	287								A5PB-12	W29 1.125" ±.0625 (SEE SHT. 2)	A6PB-12								
IB3(ECL)	288								A5PB-13		A6PB-13								
IB3(TTL)	289								A5PB-14		A6PB-14								
IB4(ECL)	290								A5PB-15		A6PB-15								
IB4(TTL)	291								A5PB-16		A6PB-16								
IB5(ECL)	292								A5PB-17		A6PB-17								
IB5(TTL)	293								A5PB-18		A6PB-18								
IB6(ECL)	294								A5PB-19		A6PB-19								
IB6(TTL)	295								A5PB-20		A6PB-20								
IB7(ECL)	296								A5PB-21		A6PB-21								
IB7(TTL)	297								A5PB-22		A6PB-22								
TRUE PATTERN	298								A5PB-23		A6PB-23								
$\overline{W7}$	299								A5PB-24		A6PB-24								
P1	300				-	GRAY	-	#7	A5PB-25		A6PB-25				-	GRAY	-	#7	A6JB-25
A5JB-25																			

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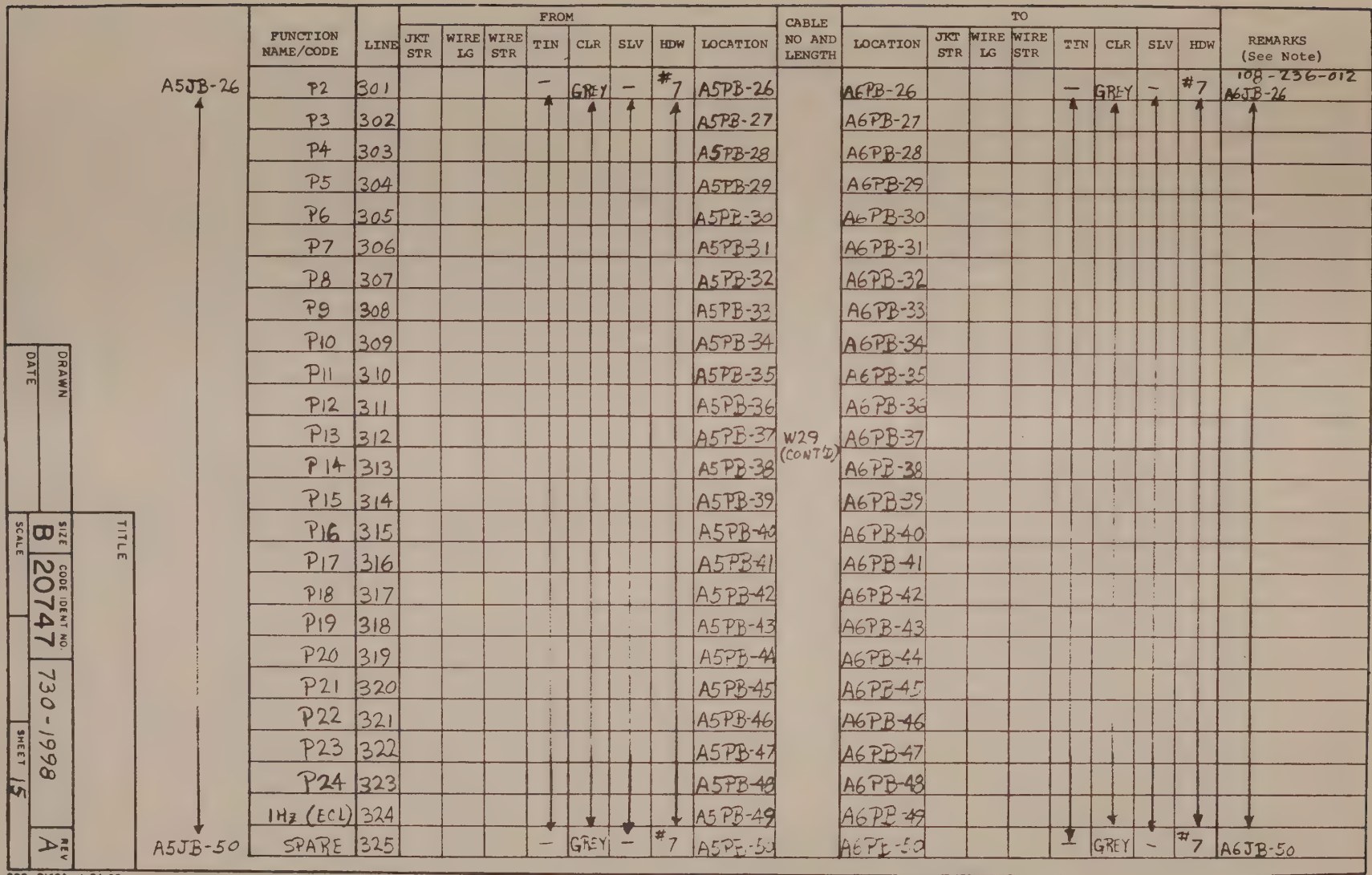
Figure 6-12. Model 607 Chassis Wire List (sheet 14)



	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A5JB-26	P2	301				—	GREY	—	#7	A5PB-26		A6PB-26				—	GREY	—	#7	108-236-012 A6JB-26
	P3	302								A5PB-27		A6PB-27								
	P4	303								A5PB-28		A6PB-28								
	P5	304								A5PB-29		A6PB-29								
	P6	305								A5PB-30		A6PB-30								
	P7	306								A5PB-31		A6PB-31								
	P8	307								A5PB-32		A6PB-32								
	P9	308								A5PB-33		A6PB-33								
	P10	309								A5PB-34		A6PB-34								
	P11	310								A5PB-35		A6PB-35								
	P12	311								A5PB-36		A6PB-36								
	P13	312								A5PB-37	W29 (CONT'D)	A6PB-37								
	P14	313								A5PB-38		A6PB-38								
	P15	314								A5PB-39		A6PB-39								
	P16	315								A5PB-40		A6PB-40								
	P17	316								A5PB-41		A6PB-41								
	P18	317								A5PB-42		A6PB-42								
	P19	318								A5PB-43		A6PB-43								
	P20	319								A5PB-44		A6PB-44								
	P21	320								A5PB-45		A6PB-45								
	P22	321								A5PB-46		A6PB-46								
	P23	322								A5PB-47		A6PB-47								
	P24	323								A5PB-48		A6PB-48								
	1Hz (ECL)	324								A5PB-49		A6PB-49								
A5JB-50	SPARE	325				—	GREY	—	#7	A5PB-50		A6PB-50				—	GREY	—	#7	A6JB-50

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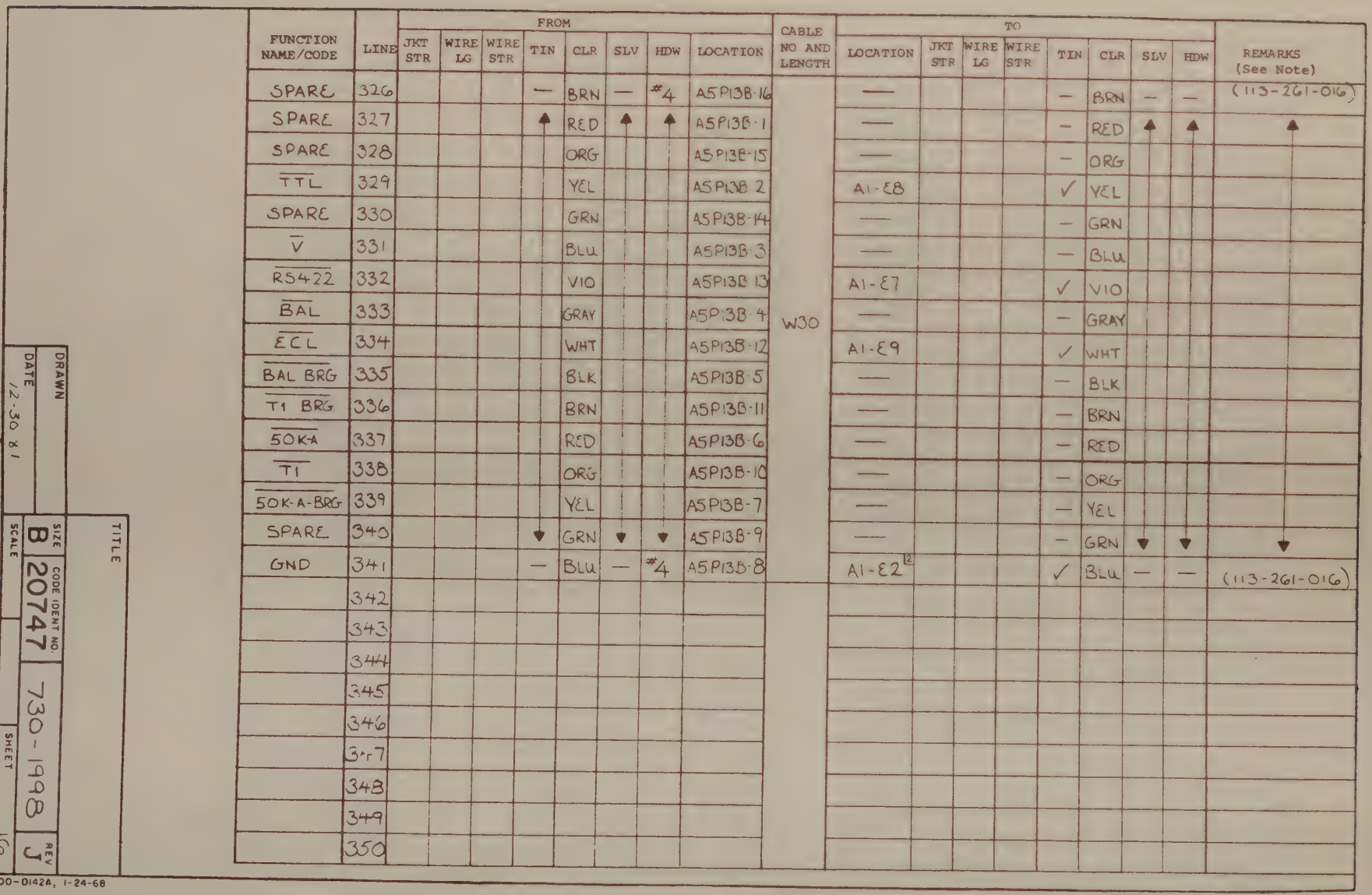
Figure 6-12. Model 607 Chassis Wire List (sheet 15)



FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
SPARE	326				—	BRN	—	#4	A5P13B-16		—				—	BRN	—	—	(113-261-016)
SPARE	327				↑	RED	↑	↑	A5P13B-1		—				—	RED	↑	↑	↑
SPARE	328					ORG			A5P13E-15		—				—	ORG			
$\overline{TTL}$	329					YEL			A5P13B-2		A1-E8				✓	YEL			
SPARE	330					GRN			A5P13B-14		—				—	GRN			
$\overline{V}$	331					BLU			A5P13B-3		—				—	BLU			
$\overline{RS422}$	332					VIO			A5P13B-13		A1-E7				✓	VIO			
$\overline{BAL}$	333					GRAY			A5P13B-4	W30	—				—	GRAY			
$\overline{ECL}$	334					WHT			A5P13B-12		A1-E9				✓	WHT			
$\overline{BAL\ BRG}$	335					BLK			A5P13B-5		—				—	BLK			
$\overline{T1\ BRG}$	336					BRN			A5P13B-11		—				—	BRN			
$\overline{50K-A}$	337					RED			A5P13B-6		—				—	RED			
$\overline{T1}$	338					ORG			A5P13B-10		—				—	ORG			
$\overline{50K-A-BRG}$	339					YEL			A5P13B-7		—				—	YEL			
SPARE	340				↓	GRN	↓	↓	A5P13B-9		—				—	GRN	↓	↓	↓
GND	341				—	BLU	—	#4	A5P13B-8		A1-E2[12]				✓	BLU	—	—	(113-261-016)
	342																		
	343																		
	344																		
	345																		
	346																		
	347																		
	348																		
	349																		
	350																		

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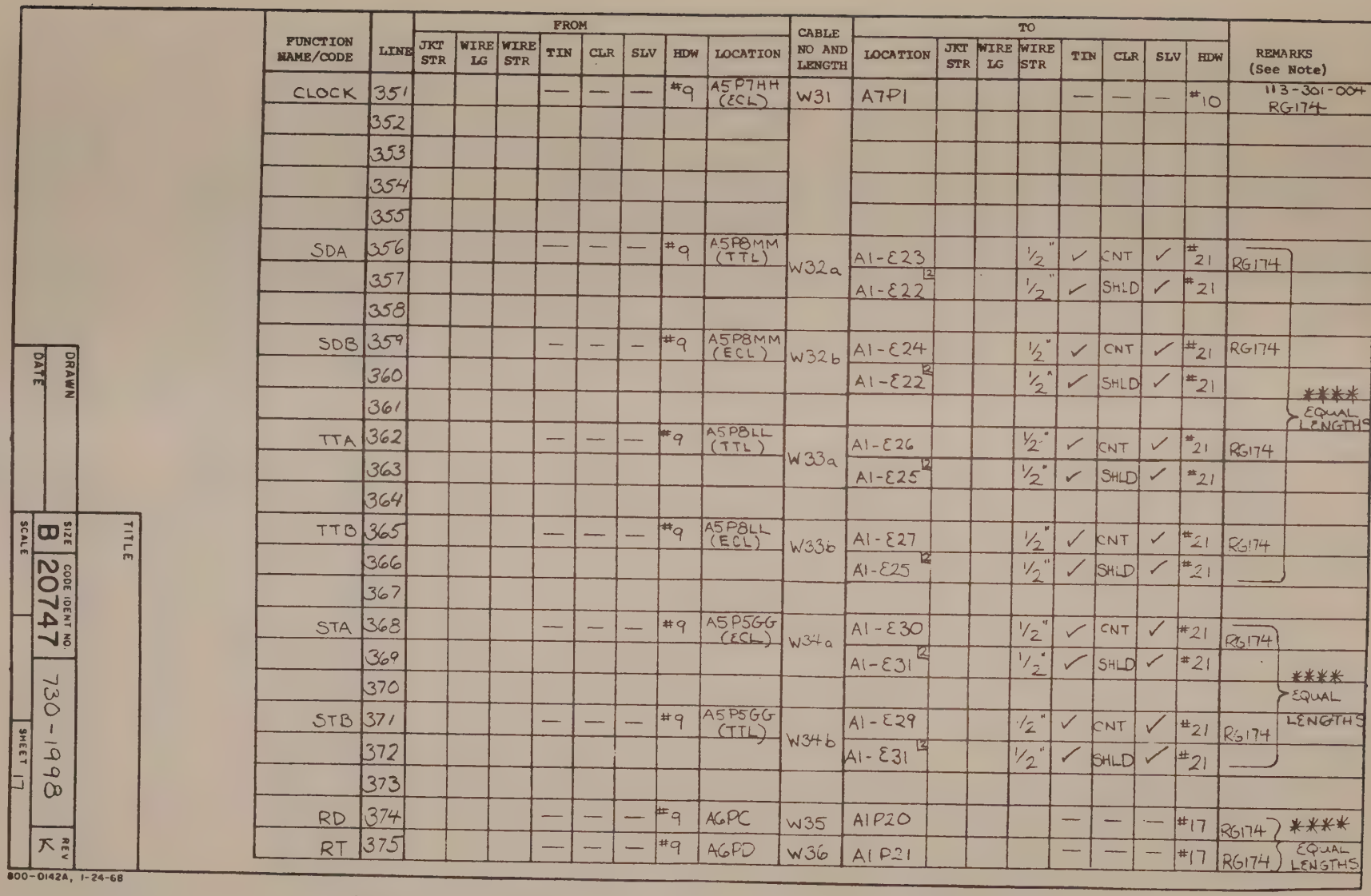
Figure 6-12. Model 607 Chassis Wire List (sheet 16)



FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
CLOCK	351				—	—	—	#9	A5P7HH (ECL)	W31	A7P1				—	—	—	#10	113-301-004 RG174
	352																		
	353																		
	354																		
	355																		
SDA	356				—	—	—	#9	A5P8MM (TTL)	W32a	A1-E23			½"	✓	CNT	✓	#21	RG174
	357										A1-E22 [2]			½"	✓	SHLD	✓	#21	
	358																		
SDB	359				—	—	—	#9	A5P8MM (ECL)	W32b	A1-E24			½"	✓	CNT	✓	#21	RG174
	360										A1-E22 [2]			½"	✓	SHLD	✓	#21	**** EQUAL LENGTHS
	361																		
TTA	362				—	—	—	#9	A5P8LL (TTL)	W33a	A1-E26			½"	✓	CNT	✓	#21	RG174
	363										A1-E25 [2]			½"	✓	SHLD	✓	#21	
	364																		
TTB	365				—	—	—	#9	A5P8LL (ECL)	W33b	A1-E27			½"	✓	CNT	✓	#21	RG174
	366										A1-E25 [2]			½"	✓	SHLD	✓	#21	
	367																		
STA	368				—	—	—	#9	A5P5GG (ECL)	W34a	A1-E30			½"	✓	CNT	✓	#21	RG174
	369										A1-E31 [2]			½"	✓	SHLD	✓	#21	**** EQUAL LENGTHS
	370																		
STB	371				—	—	—	#9	A5P5GG (TTL)	W34b	A1-E29			½"	✓	CNT	✓	#21	RG174
	372										A1-E31 [2]			½"	✓	SHLD	✓	#21	
	373																		
RD	374				—	—	—	#9	A6PC	W35	A1P20				—	—	—	#17	RG174 ****
RT	375				—	—	—	#9	A6PD	W36	A1P21				—	—	—	#17	RG174 EQUAL LENGTHS

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730-1998
SHEET 17
REV K

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 17)

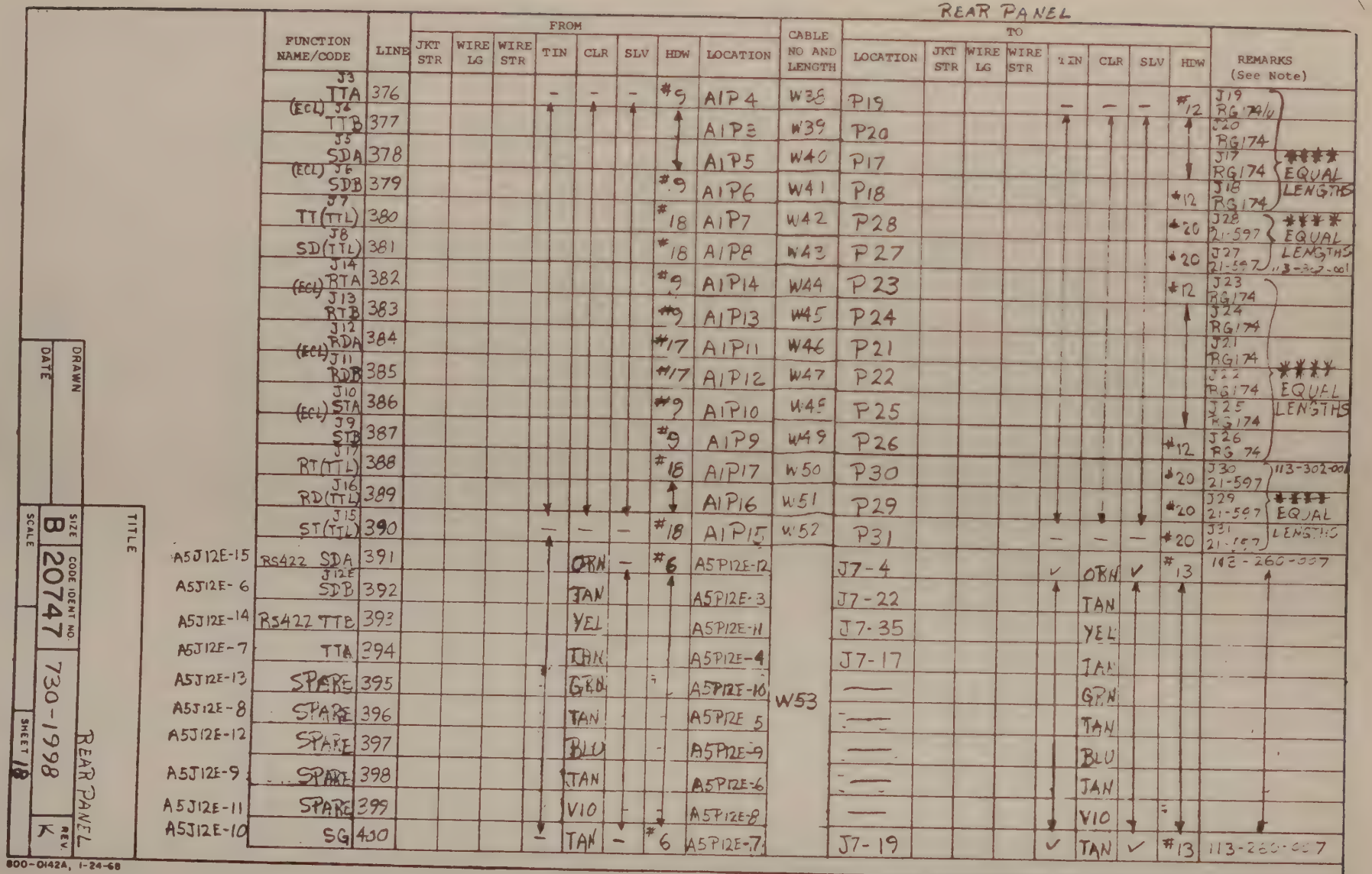

Figure 6-12. Model 607 Chassis Wire List (sheet 18)

REAR PANEL

	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
		401																		
		402																		
		403																		
A5J5X-7	BPV	404				✓	GRN	–	#14	A5P5X-6	W54	J9-1				✓	GRN	✓	#15	#26 AWG TWISTED PAIR
A5J5X-14	GND	405					BLK			A5P5X-11		J9-14					BLK			
A5J5X-8	T-PAT SYNC	406					GRN			A5P5X-7	W55	J9-2					GRN			#26 AWG TWISTED PAIR
A5J5X-13	GND	407					BLK			A5P5X-10		J9-15					BLK			
A6J5X-2	BAD BLK	408					GRN			A6P5X-1	W56	J9-7					GRN			#26 AWG TWISTED PAIR
A6J5X-19	GND	409					BLK			A6P5X-16		J9-20					BLK			
A6J5X-3	ERROR	410					GRN			A6P5X-2	W57	J9-8					GRN			
A6J5X-18	GND	411					BLK			A6P5X-15		J9-21					BLK			
A6J5X-4	REC PAT SYNC	412					GRN			A6P5X-3	W58	J9-9					GRN			
A6J5X-17	GND	413					BLK			A6P5X-14		J9-22					BLK			
A6J5X-5	RESYNC	414					GRN			A6P5X-4	W59	J9-10					GRN			
A6J5X-16	GND	415					BLK			A6P5X-13		J9-23					BLK			
A6J5X-6	ALARM	416					GRN			A6P5X-5	W60	J9-11					GRN			
A6J5X-15	GND	417					BLK			A6P5X-12		J9-24					BLK			
A6J5X-7	BLK or SEC INT	418					GRN			A6P5X-6	W61	J9-12					GRN			#26 AWG TWISTED PAIR
A6J5X-14	GND	419				✓	BLK	–	#14	A6P5X-11		J9-25				✓	BLK	✓	#15	
	RS422 RTA	420					GRN		–	A1-E14	W62	J7-8					GRN	✓	#13	
	RTB	421					BLK			A1-E13		J7-26					BLK			
	RS422 RDB	422					GRN			A1-E15	W63	J7-24					GRN			
	RDA	423					BLK			A1-E12		J7-6					BLK			
	RS422 STA	424					GRN			A1-E11	W64	J7-5					GRN			#26 AWG TWISTED PAIR
	STB	425				✓	BLK	–	–	A1-E10		J7-23				✓	BLK	✓	#13	

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SHEET 19
REV K
TITLE REAR PANEL
730-1998

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 19)

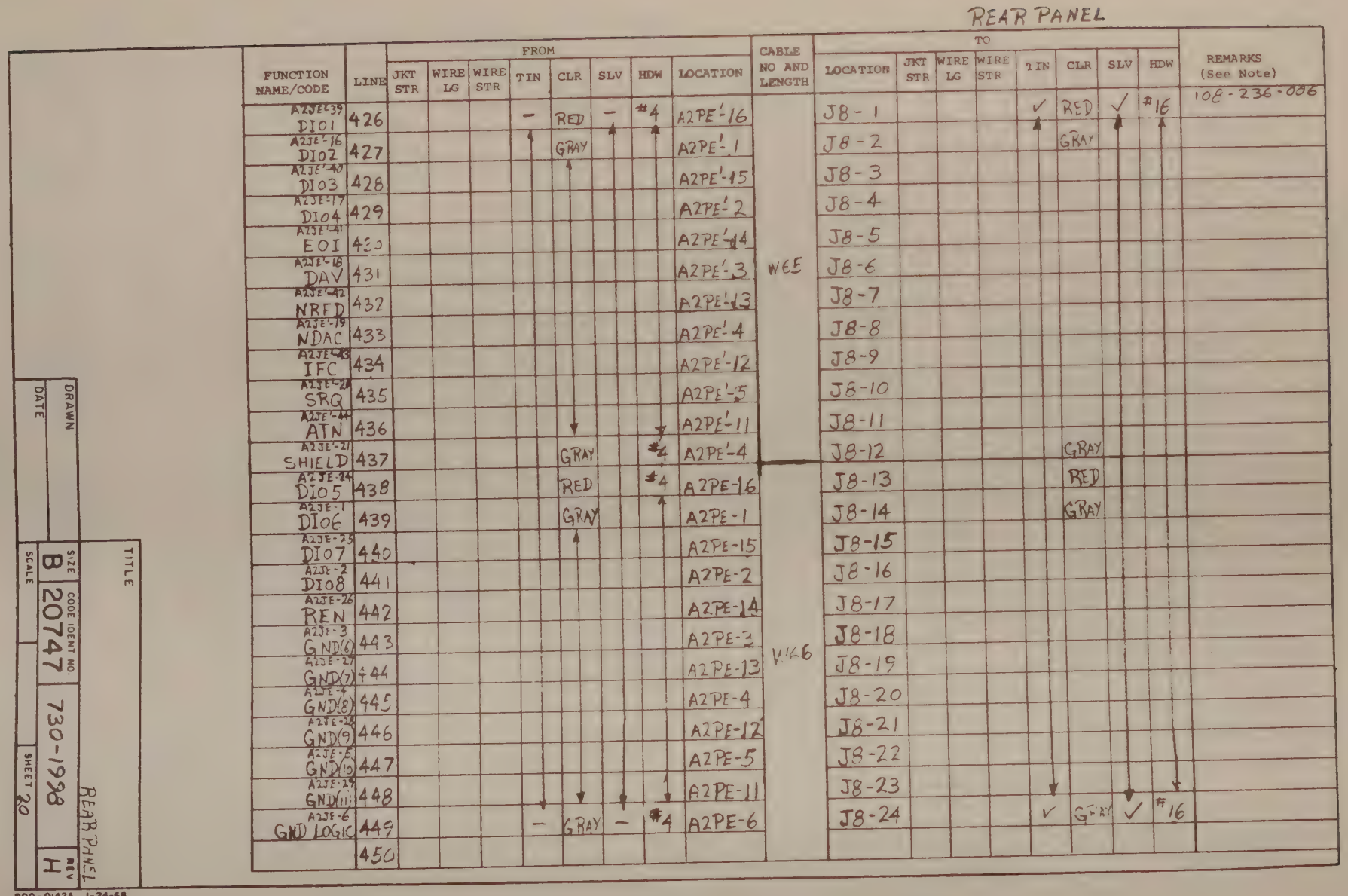
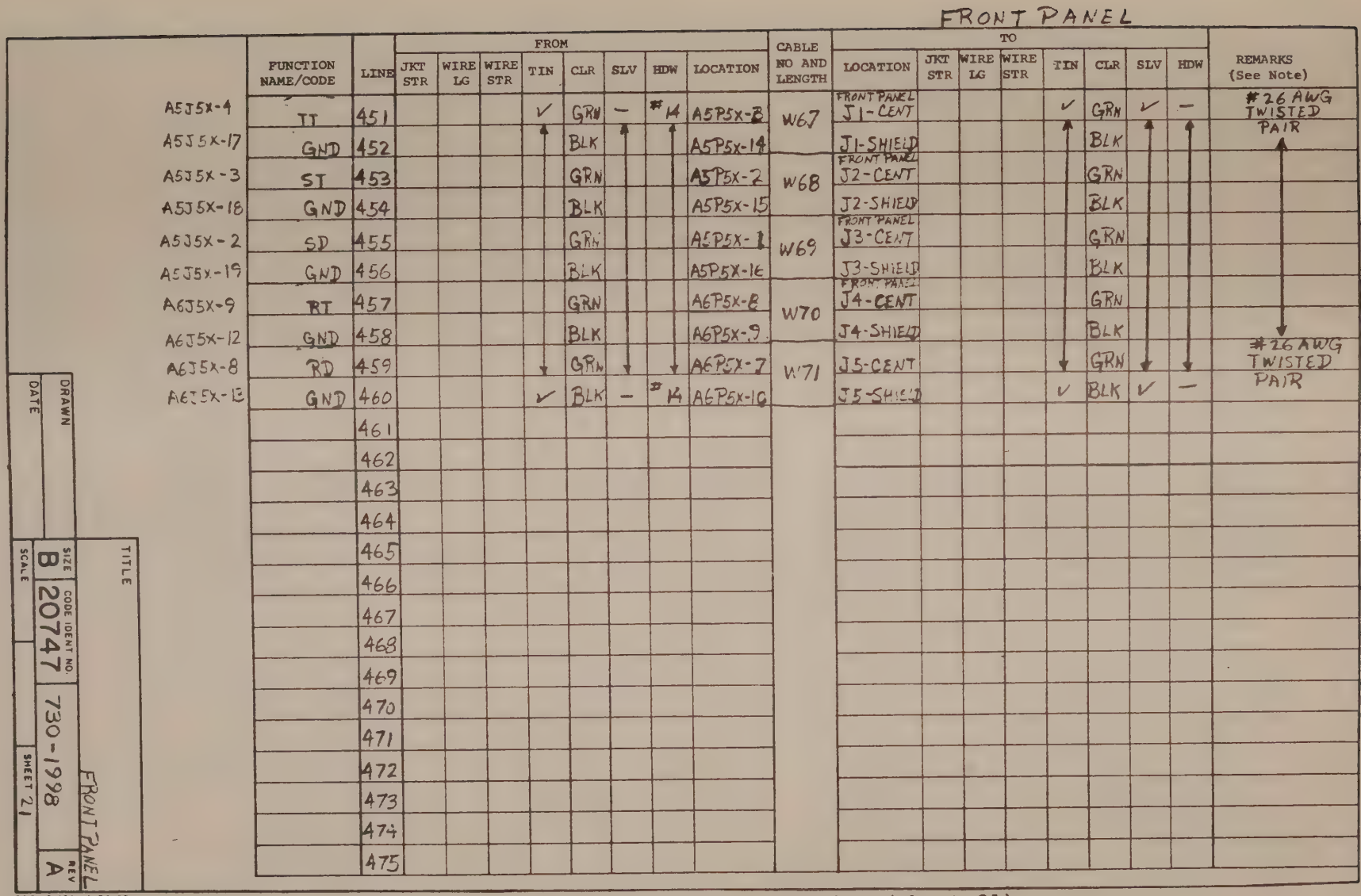


Figure 6-12. Model 607 Chassis Wire List (sheet 20)



FRONT PANEL

	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A5J5X-4	TT	451				✓	GRN	—	#14	A5P5X-2	W67	FRONT PANEL J1-CENT				✓	GRN	✓	—	#26 AWG TWISTED PAIR
A5J5X-17	GND	452					BLK			A5P5X-14		J1-SHIELD					BLK			
A5J5X-3	ST	453					GRN			A5P5X-2	W68	FRONT PANEL J2-CENT					GRN			
A5J5X-18	GND	454					BLK			A5P5X-15		J2-SHIELD					BLK			
A5J5X-2	SD	455					GRN			A5P5X-1	W69	FRONT PANEL J3-CENT					GRN			
A5J5X-19	GND	456					BLK			A5P5X-16		J3-SHIELD					BLK			
A6J5X-9	RT	457					GRN			A6P5X-8	W70	FRONT PANEL J4-CENT					GRN			
A6J5X-12	GND	458					BLK			A6P5X-9		J4-SHIELD					BLK			
A6J5X-8	RD	459					GRN			A6P5X-7	W71	J5-CENT					GRN			#26 AWG TWISTED PAIR
A6J5X-13	GND	460				✓	BLK	—	#14	A6P5X-10		J5-SHIELD				✓	BLK	✓	—	
		461																		
		462																		
		463																		
		464																		
		465																		
		466																		
		467																		
		468																		
		469																		
		470																		
		471																		
		472																		
		473																		
		474																		
		475																		

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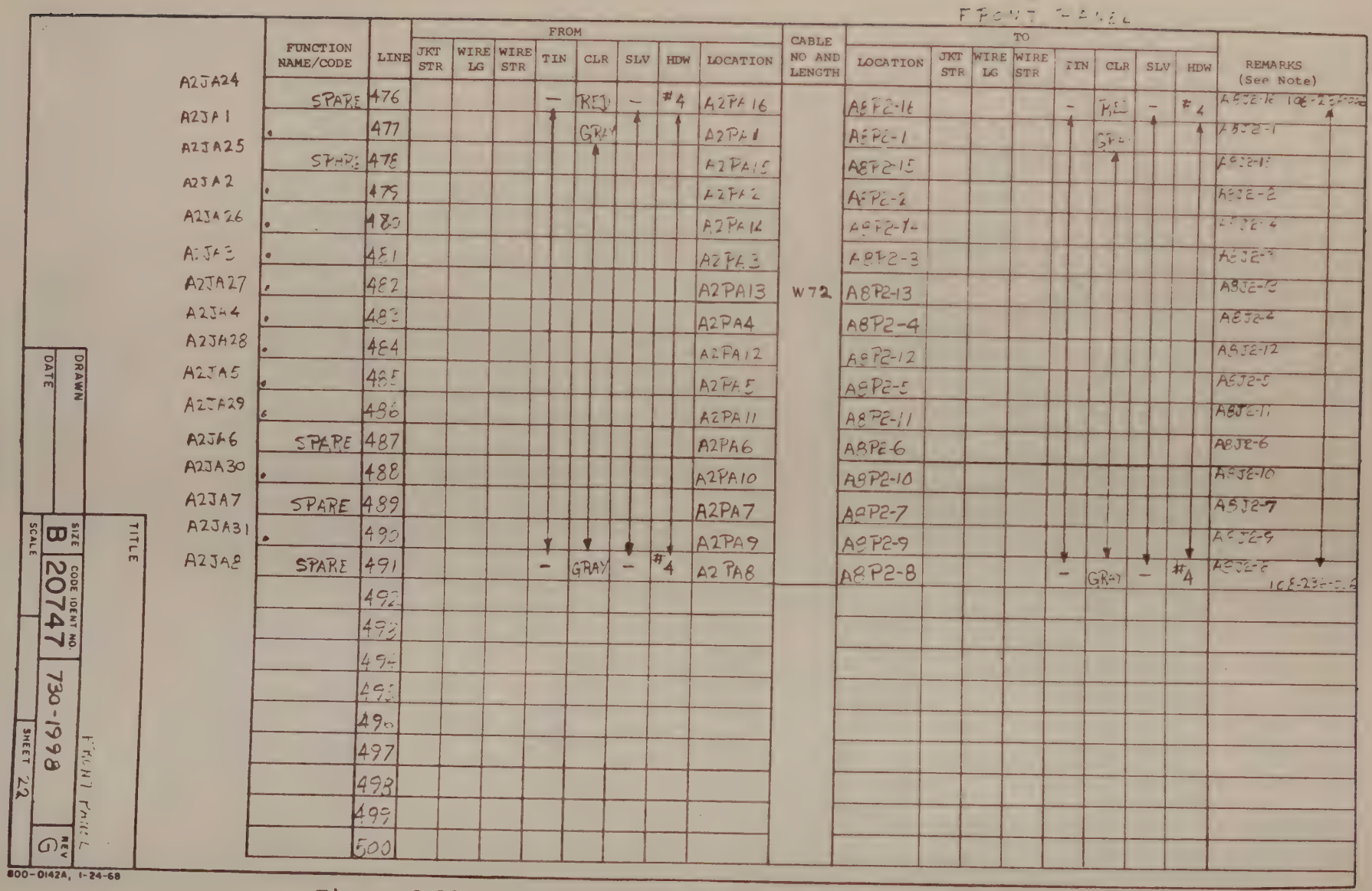
TITLE FRONT PANEL
730-1998
REV A
SHEET 21

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 21)



	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A2JA24	SPARE	476				—	RED	—	#4	A2PA16		A8P2-16				—	RED	—	#4	A8J2-16
A2JA1	"	477					GRAY			A2PA1		A8P2-1					GRAY			A8J2-1
A2JA25	SPARE	478								A2PA15		A8P2-15								A8J2-15
A2JA2	"	479								A2PA2		A8P2-2								A8J2-2
A2JA26	"	480								A2PA14		A8P2-14								A8J2-14
A2JA3	"	481								A2PA3		A8P2-3								A8J2-3
A2JA27	"	482								A2PA13	W72	A8P2-13								A8J2-13
A2JA4	"	483								A2PA4		A8P2-4								A8J2-4
A2JA28	"	484								A2PA12		A8P2-12								A8J2-12
A2JA5	"	485								A2PA5		A8P2-5								A8J2-5
A2JA29	"	486								A2PA11		A8P2-11								A8J2-11
A2JA6	SPARE	487								A2PA6		A8P2-6								A8J2-6
A2JA30	"	488								A2PA10		A8P2-10								A8J2-10
A2JA7	SPARE	489								A2PA7		A8P2-7								A8J2-7
A2JA31	"	490								A2PA9		A8P2-9								A8J2-9
A2JA8	SPARE	491				—	GRAY	—	#4	A2PA8		A8P2-8				—	GRAY	—	#4	A8J2-8
		492																		
		493																		
		494																		
		495																		
		496																		
		497																		
		498																		
		499																		
		500																		

FRONT PANEL

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SIZE B | CODE IDENT NO. 20747 | 730-1998 | REV G

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SHEET 22

TITLE FRONT PANEL

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Figure 6-12. Model 607 Chassis Wire List (sheet 22)

FRONT PANEL

	FUNCTION NAME/CODE	LINE	FROM JKT STR	FROM WIRE LG	FROM WIRE STR	FROM TIN	FROM CLR	FROM SLV	FROM HDW	FROM LOCATION	CABLE NO AND LENGTH	TO LOCATION	TO JKT STR	TO WIRE LG	TO WIRE STR	TO TIN	TO CLR	TO SLV	TO HDW	REMARKS (See Note)
A2JB 39	SPARE	501				—	RED	~	#4	A2PB 16		A8P1-16				—	RED	~	#4	A8J1-16 108-236-006
A2JB 16	"	502					GRAY			A2PB 1		A8P1-1					GRAY			A8J1-1
A2JB 40	SPARE	503								A2PB 15		A8P1-15								A8J1-15
A2JB 17	"	504								A2PB 2		A8P1-2								A8J1-2
A2JB 41	"	505								A2PB 14		A8P1-14								A8J1-14
A2JB 18	"	506								A2PB 3		A8P1-3								A8J1-3
A2JB 42	"	507								A2PB 13		A8P1-13								A8J1-13
A2JB 19	SPARE	508								A2PB 4	W73	A8P1-4								A8J1-4
A2JB 43	"	509								A2PB 12		A8P1-12								A8J1-12
A2JB 20	"	510								A2PB 5		A8P1-5								A8J1-5
A2JB 44	"	511								A2PB 11		A8P1-11								A8J1-11
A2JB 21	SPARE	512								A2PB 6		A8P1-6								A8J1-6
A2JB 45	"	513								A2PB 10		A8P1-10								A8J1-10
A2JB 22	SPARE	514								A2PB 7		A8P1-7								A8J1-7
A2JB 46	SPARE	515								A2PB 9		A8P1-9								A8J1-9
A2JB 23	SPARE	516				—	GRAY	—	#4	A2PB 8		A8P1-8				—	GRAY	—	#4	A8J1-8 108-236-006
		517																		
		518																		
		519																		
		520																		
		521																		
		522																		
		523																		
		524																		
		525																		

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SIZE B
CODE IDENT NO 20747
SCALE
SHEET 23
REV G
TITLE FRONT PANEL
730-1998

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Figure 6-12. Model 607 Chassis Wire List (sheet 23)

FUNCTION NAME/CODE	LINE	FROM								CABLE NO AND LENGTH	TO								REMARKS (See Note)
		JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	LOCATION		LOCATION	JKT STR	WIRE LG	WIRE STR	TIN	CLR	SLV	HDW	
$\overline{CTS}$	526					GRAY			A2FD43-8		REAR PANEL J6-4					GRAY			
DCD	527					GRAY			A2FD43-9		REAR PANEL J6-20					GRAY			
$\overline{DTR}$	528					GRAY			A2FD43-11	W75	REAR PANEL J6-8					GRAY			
$\overline{RTS}$	529					GRAY			A2FD43-13		REAR PANEL J6-5					GRAY			
$\overline{TXD}$	530					GRAY			A2FD43-16		REAR PANEL J6-3					GRAY			
	531																		
	532																		
	533																		
	534																		
NMI	535				✓	RED	—	—	A9-E8		A2PD16				—	RED	—	#4	108-236-006 A2JD24
GND	536				↓	GRAY	↓	↓	A9-E9		A2PD1				↓	GRAY	↓	↓	A2JD1
A1	537					↓			A9-E1		A2PD15					↓			A2JD25
ADR	538								A9-E7		A2PD2								A2JD2
A3	539								A9-E3		A2PD14								A2JD26
A2	540								A9-E2	W74	A2PD3								A2JD3
A5	541				↓		↓	↓	A9-E5		A2PD13								A2JD27
A4	542				✓		—	—	A9-E4		A2PD4								A2JD4
	543										A2PD12								A2JD28
TO	544				✓		—	—	A9-E6		A2PD5								A2JD5
	545										A2PD11								A2JD29
	546										A2PD6								A2JD6
	547										A2PD10								A2JD30
	548										A2PD7								A2JD7
	549					↓					A2PD9				↓	↓	↓	↓	A2JD31
	550					GRAY					A2PD8				—	GRAY	—	#4	A2JD8

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SIZE B | CODE IDENT NO 20747 | 7730-1998 | REV L

SCALE

SHEET 24

TITLE

800-0142A, 1-24-68

Figure 6-12. Model 607 Chassis Wire List (sheet 24)

GLOSSARY OF MNEMONICS

A	
AB	Address Bus
ADDERR	Add Error
ADRS	Address
ALWRSE	Allow Resync
ARDY	A Ready
B	
B-ERR PROB	Bit Error Probability
BAD BLK	Bad Block
BBMON	Bad Block Monitor
BBSCLK	Bad Block Seconds Clock
BER	Bit Error Rate
BER TEST INT	Bit Error Rate Test Interval
BIT CKT	TTL Bit Clock
BIT ERR ALARM THRS	Bit Error Alarm Threshold
BIT ERRS	Bit Errors
BITCKE	ECL Bit Clock
BITMDE	ECL Bit Mode
BITMDT	TTL Bit Mode
BITTC	Bit Terminal Count
BKSCLK	Block/Seconds Clock
BLINT	Block Interval
BLK ERRS	Block Errors
BLK LN	Block Length
BLK THRUPUT	Block Throughput
BLK/SEC INT	Block/Seconds Interval
BSTB	B Strobe
BTSCLK	Bit/Seconds Clock
BUSACK	Bus Acknowledge
BUSRQ	Bus Request
C	
CB	Control Bus
CGROM	Character Generator Read-Only Memory
CNT	Control
CNTACK	Control Acknowledge
CNTEST	Control Test
CNTRDY	Control Ready
CR	Carriage Return
CRT	Cathode Ray Tube
CTC	Clock Timing Control
D	
DATARDY	Data Ready
DAV	Data Available
DB	Data Bus
DMA	Direct Memory Access
DTTS	Data Transmission Test Set

E	
ECLIB	ECL Input Bus
ECLOB	ECL Output Bus
ECLRST	ECL Reset
ENSUPO	Enable Suppression of Zero
EOI	End of Input
EOTT	End of Test Time
ERR	Error
ERRDST	Error Read Status
ERRINT	Error Interval
EXTTT	External Transmitted Timing
F	
F-0	Force Zeros
F-1	Force Ones
G	
GBGATE	Good Block Gate
H	
HD	Horizontal Drive
I	
INCR	Increment
INT	Interrupt
INT ENABLE	Interrupt Enable
INTFC	Interface
INTLK	Interlock
INVRT	Invert
IORQ	Input/Output Request
L	
LDWD	Load Word
LOOPTEST	Loop Test
LPBK	Loop Back
LTEN	Light Enable
M	
MAN	Manual
MEM	Memory
MRE	Memory Read
MRQ	Memory Request
MRT	Memory Write
N	
NDAC	Not Data Accepted
NOR	Normal
NRFD	Not Ready for Data
NVRAM	Nonvolatile Random Access Memory
NVRAM ENA	Enable Nonvolatile Random Access Memory

P

PAT LEN	Pattern Length
PAT TYPE	Pattern Type
PE	Predictor Errors
PEGT32	Predictor Errors Greater than 32
PIO	Parallel Input/Output Interface
PN	Pseudorandom Noise
PR	Pseudorandom
PR-R	Print Test Results
PR-REV	Pseudorandom Reverse
PR-S	Print Setup Parameters
PREDAT	Predict Data
PROM	Programmable Read-Only Memory

R

R/P	Recirculate Pattern
RAM	Random Access Memory
RAM A ENA	Enable Random Access Memory A
RAM B ENA	Enable Random Access Memory B
RAM C ENA	Enable Random Access Memory C
RAM D ENA	Enable Random Access Memory D
RD	Receive Data
RDA	Receive Data A
RDB	Receive Data B
RDY	Ready
RECIRC	Recirculate
REFDAT	Reference Data
ROM A ENA	Enable Read-Only Memory A
ROM B ENA	Enable Read-Only Memory B
ROM C ENA	Enable Read-Only Memory C
ROM D ENA	Enable Read-Only Memory D
ROM DCD	Read-Only Memory Decode
RPATSY	Receive Pattern Sync
RSL	Resync Logic
RSNMON	Resync Monitor
RSTRY	Resync Try
RSYFLG	Resync Flag
RT	Receive Timing
RTA	Receive Timing A
RTB	Receive Timing B
RVV	Reverse Video

S	
SBI0 - SBI7	Select Block Interval 0-7
SD	Send Data
SDA	Send Data A
SDB	Send Data B
SDMON	Send Data Monitor
SEC ERRS	Seconds Errors
SEC THRUPUT	Seconds Throughput
SECS	Seconds
SEL50K	Select 50kb
SF0-SF19	Select Frequency 0 through Select Frequency 19
SL0-SL3	Select Length 0 through Select Length 3
SLFTST	Self-Test
SLHIRT	Select High Rate
SO0-SO2	Select Oscillator 0 through Select Oscillator 2
SPATSY	Send Pattern Sync
ST	Send Timing
STA	Send Timing A
STB	Send Timing B
STMON	Send Timing Monitor
SYNLD	Sync Load
SYNPLS	Sync Pulse
T	
THRPUT TST INT	Throughput Test Interval
THRS	Threshold
TO	Talk Only
TRUPAT	True Pattern
TSTLN	Test Length
TT	Terminal Timing
TTA	Terminal Timing A
TTB	Terminal Timing B
TTLIB	TTL Input Bus
TTLOB	TTL Output Bus
TTMON	Terminal Timing Monitor
TXER	Transmitter Error Rate
TXPOL	Transmitter Polarity
V	
VB	Vertical Blanking
VD	Vertical Drive
VSP	Video Suppression
W	
W/R	Write/Read
WR	Write

APPENDIX A

POWER SUPPLIES

A-1 GENERAL

This section contains manufacturer's specifications and information for the power supplies used in the Model 607 DTTS. PS1 is a Model DS150-301. PS2 is a Model SK5-40/OVP.

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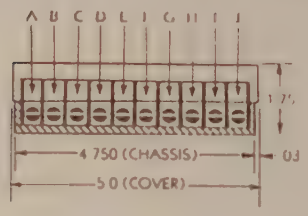
MECHANICAL SPECIFICATIONS

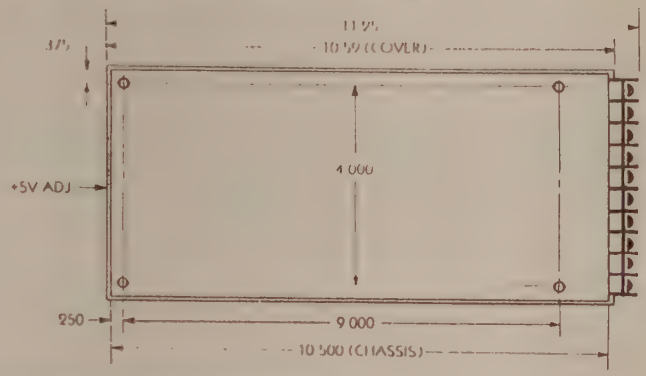
TOLERANCES
XX = ± .03
XXX = ± .015

MOUNTING
8 .32 PEM NUT
(4 HOLES)

CHASSIS
.100" GA. ALUMINUM

WEIGHT RANGE
3.25 - 3.50 POUNDS





MODEL OUTPUT CONFIGURATION

Keyed to terminal diagram above

OUTPUT*	A	B	C	D	E	F	G	H	I	J
SINGLE OUTPUT (Standard)	AC	AC	CHASSIS	NO CONN	COM.	COM.	-S	+S	A	A
DUAL OUTPUT (Standard)	AC	AC	CHASSIS	AUX. B	COM.	COM.	-S	+S	A	A
TRIPLE OUTPUT (Standard)	AC	AC	CHASSIS	AUX. B	AUX. C	NO CONN	COM	COM	A	A

*See Rating Chart for specific model outputs

STANDARD MODELS, 115VAC INPUT

OUTPUT TERMINAL SINGLE	I,J A	DUAL	D AUX. B	I,J A
DS 150-105	5V @ 30A	DS 150-201	+12V @ 4A	+5V @ 30A -003
112	12V @ 12A	202	-28V @ 3A	+28V @ 3A
115	15V @ 10A	203	-5V @ 1A	+5V @ 24A
124	24V @ 6A	204	-12V @ 4A	+12V @ 8A
128	28V @ 5A	207	-5V @ 5A	5V @ 25A
148	48V @ 3A	208	24V @ 1.5A	12V @ 10A
		209	-18V @ 3A	18V @ 3A
		211	-15V @ 3A	15V @ 3A

	OUTPUT TERMINAL TRIPLE	D AUX. B	E AUX. C	I,J A
-001	DS 150-301	12V @ 4A	-12V @ 1A	5V @ 24A
	302	12V @ 3A	-12V @ 3A	5V @ 24A
	304	15V @ 3A	-15V @ 3A	5V @ 24A
	310	+12 @ 5A	-5V @ 2A	5V @ 15A
	315	28V @ 2.5A	-5V @ 2A	5V @ 15A
	316	16.5V @ 3A	-16.5V @ 3A	5V @ 24A
	321	12V @ 3A	+24V @ 3A	5V @ 20A
	322	-28V @ 2.5A	-5V @ 2A	5V @ 15A

136-120-□
SHEET 2

SP 250 } SERIES
SP 252 }

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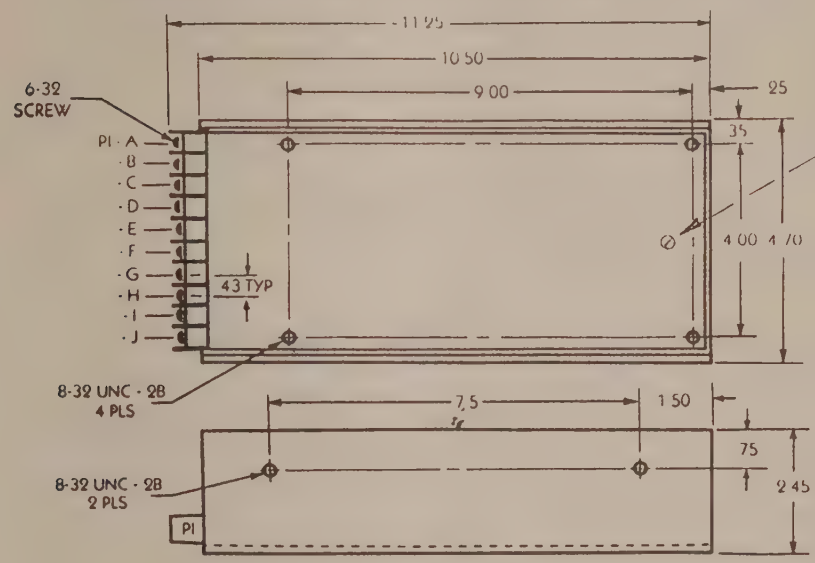
MECHANICAL SPECIFICATIONS



TERMINAL*	A	B	C	D	E	F	G	H	I	J
SINGLE OUTPUT (Standard)	AC	AC	CHASSIS	NO CONN	COM.	COM.	-S	+S	A	A
DUAL OUTPUT (—201)	AC	AC	CHASSIS	AUX. B	COM	COM	-S	+S	A	A
TRIPLE OUTPUT (Standard)	AC	AC	CHASSIS	AUX. B	AUX. C	NO CONN	COM	COM	A	A

*See Rating Chart for specific model outputs

AMS PART NO.	MODEL NUMBER	OUTPUT A TERMINAL "I","J"	OUTPUT B TERMINAL "D"	OUTPUT C TERMINAL "E"	INPUT VOLTAGE
-004	SP252-217	-5V@ 40A	-2V@ 20A	—	115/230 VAC

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SELECTION GUIDE

SERIES	OUTPUT POWER (WATTS)	INPUT VOLTAGE (V.A.C.)	NOTES	TYPE	PAGE
DU50—	50	115/230	3	OPEN FRAME	1, 2, 3
DU65—	65	115/230	4	OPEN FRAME	
DS150—	150	115	—	ENCLOSED	
DS152—	150	230	—	ENCLOSED	
DS160—	150	115	—	ENCLOSED	
DS161—	150	115	1, 2	ENCLOSED	4, 5
DS162—	150	230	—	ENCLOSED	6, 7
DS163—	150	230	1, 2	ENCLOSED	
HU200—	200	115/230	1	OPEN FRAME	8, 9
*HU210—	200	115/230	1	OPEN FRAME	
DU250—	250	115	—	OPEN FRAME	10, 11
DU252—	250	230	—	OPEN FRAME	12
DU260—	250	115	—	OPEN FRAME	
DU261—	250	115	1, 2	OPEN FRAME	INSIDE
DU262—	250	230	—	OPEN FRAME	BACK
DU263—	250	230	1, 2	OPEN FRAME	COVER

1. WITH POWER FAIL.
2. REMOTE SHUT-OFF OPTIONAL.
3. BOSCHERT OL50 EQUIVALENT.
4. BOSCHERT OL65 EQUIVALENT.

*HU210: All outputs regulated. For specifics consult factory.

GENERAL SPECIFICATIONS

SHOCK AND VIBRATION:

The Power Supply will withstand without degradation any reasonable shock and vibration found in the normal course of storage and operation when properly packaged, handled and installed. This includes transportation by a commercial carrier and operation in a non-mobile mainframe.

TEMPERATURE COEFFICIENTS OF OUTPUTS

+5V: 0.02%/°C Typ.
Other Outputs: 0.05%/°C Typ.

RELATIVE HUMIDITY RANGE

Non-Condensing: 20% to 80%

ALTITUDE

Operating: 10,000 FT.
Non-Operating: 30,000 FT.

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SPECIFICATIONS

AC INPUT: Standard dual range: 90-130 VAC or 180-260 VAC, 47-63 Hz., single phase. Voltage range selectable at input barrier strip, no jumpers required.

BROWN-OUT PROTECTION: Regulation is maintained down to 90/180 VAC, at full load, with no compromise in performance.

CARRYOVER TIME: 20msec minimum after AC input voltage is lost. Carryover time is measured at full load and nominal input line conditions.

EFFICIENCY: 75% minimum at full load over entire AC input voltage range.

DC OUTPUT RATINGS: 5.0 VDC at 40A. Adjustable ± 10%. 200 watts maximum continuous output power.

REGULATION CHARACTERISTICS: Line: ± 0.1% for a full line change of 90-130 VAC or 180-260 VAC. Load: ± 0.1% for a 100% load change.

OUTPUT RIPPLE AND NOISE (PARD):
Source component: <10mv PK-PK maximum.
Switching component: <40mv PK-PK maximum.

STABILITY: Output voltage changes less than 0.1% for 24 hours following an initial 30 minute warmup period.

TEMPERATURE COEFFICIENT: ± .01% / °C maximum, over entire operating temperature range of 0° C to + 70° C.

TRANSIENT RESPONSE: For recovery to within 1% of nominal voltage set point.
Recovery time: 150 μ sec typical, 200 μ sec maximum.
Maximum voltage deviation: 5% from nominal voltage set point.

REMOTE SENSING: Remote sensing capabilities are provided to compensate for load lead losses of up to 0.5V total. Open sense lead protection is provided.

REMOTE VOLTAGE PROGRAMMING: An external resistance may be used to program output voltage. Program resistance is 1000 Ω/volt.

REMOTE SHUTDOWN: Isolated terminals are provided for remote on-off control of DC output. 5ma required for shutdown.

POWER FAIL WARNING SIGNAL: TTL compatible output sinks 5ma to the negative sense terminal when DC output is present. Goes high 2 msec before DC output drops out of regulation.

OUTPUT OVERLOAD PROTECTION: Overload protection limits output to 105-125% of full rated current.

Upon short circuit, output is automatically reduced to less than 25% of full rated current after (1) second.
Overload protection is reset by removing the short circuit and cycling AC input voltage.

OVERVOLTAGE PROTECTION: Adjustable OVP shutdown is factory preset at 120-130% of nominal output voltage set point. OVP is reset by cycling AC input voltage.

REVERSE VOLTAGE PROTECTION: Inherently protected from damage due to application of reverse polarity voltage across DC output terminals.

INPUT PROTECTION: AC input line fuse provided. Internally located.

TURN-ON TIME: 100 msec maximum after application of AC power. No overshoot on turn-on or turn-off.

OPERATING FREQUENCY: Constant 28KHz nominal.

TEMPERATURE RATINGS: Operating: 0° C to + 50° C at full output current. Consult factory for operating information for operation between + 50° C to + 70° C. Storage: – 55° C to + 85° C.

COOLING: Convection cooling is adequate where non-restricted airflow is available. When operating in a confined area, moving air or conduction cooling is recommended.

VIBRATION: Per Mil-Std-810B, Method 514, Procedure I, Curve AB (to 50Hz).

SHOCK: Per Mil-Std-810B, Method 516, Procedure V.

DIMENSIONS:

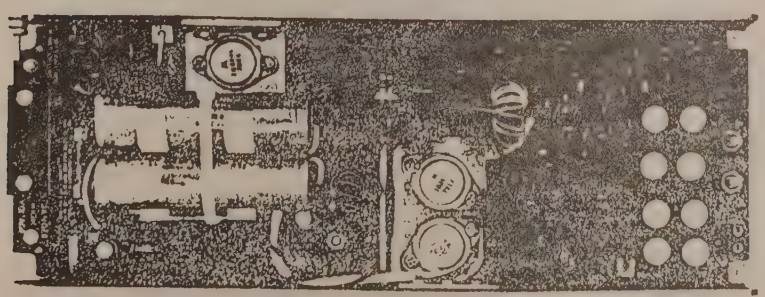
	Length	Width	Height	Weight	Volume
English	13.00"	4.88"	2.00"	3 lb./14oz	127 C.I.
Metric	330.2MM	123.9MM	50.8MM	1.76 KG	2060 C.C.

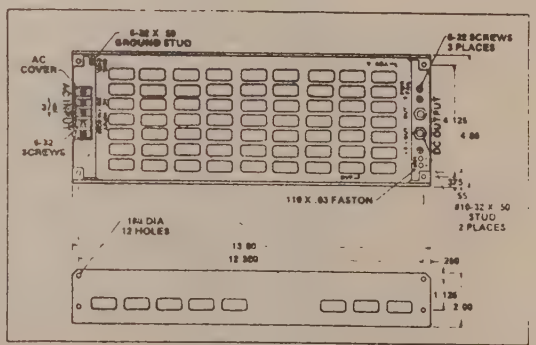
MOUNTING PROVISIONS: Mounting on 3 main chassis surfaces. (4) .188 through holes provided on each surface.

INPUT/OUTPUT TERMINATIONS:
Input: Barrier strip with protective cover. #6-32 screw terminals centered on .375" spacings. A dedicated #6-32 x .50" stud is provided for grounding.
Output: DC power output: 10-32 x .5" studs.
Remote Sense and Power Fail Signal: #6-32 screw terminals.

CONSTRUCTION: All aluminum chassis and safety cover. Clear anodize finish.

ISOLATION:
Input to Output: 2500 VAC RMS;
Input to Chassis: 1500 VAC RMS;
Output to Chassis: 500 VDC.





Power-One INC
D.C. POWER SUPPLIES
Power-One Drive • Camarillo, CA 93010 • (805) 484-2806 • TWX: 910-336-1297

HOLDSWORTH & CO.
Sales Engineer
Box 298, Newtown Square, PA 190
215 356-2350

136-116-001

POWER-ONE, INC.
DC POWER SUPPLIES

APPLICATION DATA
Including:
1. Block Diagram
2. Specification
3. Outline & Mounting Drawing
4. General User Information

Model
SK5-40/OVP
SWITCHING POWER SUPPLY

SPECIFICATIONS:

AC Input: 90-130 or 180-260 VAC, 47-440 Hz.

Input Fusing: 3AG 5A.

DC Output 5.0V adjustable ±5%.

Line Regulation: ±0.1% over specified AC input range.

Load Regulation: ±0.1% for 100% load change.

Output Ripple: 50mV PP maximum.

Transient Response: 200usec to 0.5% final value for 50% load change at nominal line. Maximum deviation 250mV.

Short-Circuit or Overload Protection: Current limit at 105-125% full load. Short circuit current <10A after 1 second.

OVP: 6.2V adjustable.

Reverse Voltage Protection: Inherent in output rectifiers.

Cooling: Convection cooled in free air. Must be forced-air cooled or derated when confined.

Temperature Rating: Full power at 0-50°C, derate linearly to 40% at 70°C (free-air temperature).

Carryover Time: 20msec minimum after loss of input at full load and nominal line.

Efficiency:, 75% minimum at full load over specified input voltage range.

Temperature Coefficient: ±.01%/°C maximum over 0-70°C operating temperature range.

Stability: 0.1% maximum change for 24-hour after 30-min warmup.

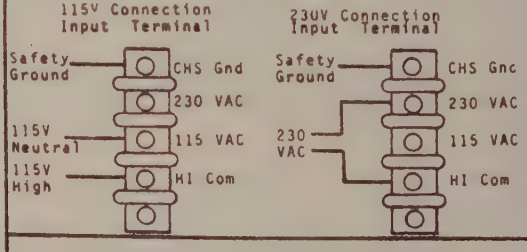
Vibration: Per Mil-Std 810B Method 514, Procedure I, curve AB (to 50Hz).

Shock: Per Mil-Std 810B Method 516, Procedure V.

Weight: 3 pounds, 14 ounces.

APPLICATION NOTES

Input Connections
Either the 115V or the 230V range can be selected by simply connecting the line to the appropriate terminals. No jumpers are required.



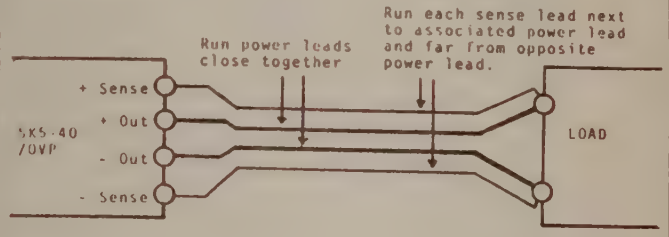
Output Connections
Output connections are by #10 lug. A minimum wire size of #9 AWG may be used for loads up to 3 feet from the supply.

Remote Sense
Terminals are provided for remote sensing. When remote sensing is used, the straps connecting the sense terminals to the output terminals must be removed. Internal resistors connecting the output and sense terminals prevent output overvoltage if a sense lead is disconnected.

Most power supply stability problems associated with remote sensing operation can be avoided by proper lead routing. The two leads connecting the output to the load must always be run together as close as possible to minimize series lead inductance.

For long cable runs, the arrangement shown below is preferred. For shorter distances, simply twisting the load leads together and the sense leads together is usually enough.

Recommended Lead Routing for Remote Sense Operation



Power Fail Output
The power fail output is a transistor with its collector uncommitted. It can sink three TTL loads or 6mA to the negative sense terminal. This signal is low during normal operation. When the input voltage falls below minimum, the signal goes high to indicate a minimum of two milliseconds of storage remaining before dropout. After the output drops out of regulation, the power fail signal may or may not be present. For this reason, to prevent false indication when the power fail signal is used by circuitry other than that which the supply is powering, it should be combined with a signal which senses that the power supply output is present.

Inhibit
The supply can be totally shut down by passing a current through the two isolated inhibit terminals. The inhibit circuit is TTL compatible; with the inhibit + terminal connected to a 5V logic supply, a TTL low on the inhibit - terminal will shut down the power supply. The resistance between terminals is 1K ohm, and 4mA minimum is required to inhibit the supply. Maximum input current is 20mA (at 20V).

Output Voltage and OVP Adjustments

The output voltage and OVP firing voltage are both adjustable by means of potentiometers on the output PC board. Refer to the Outline & Mounting Drawing for the locations of these adjustments.

CAUTION: HIGH VOLTAGES INSIDE. Use insulated tools when making voltage or OVP adjustments. Wait 5 minutes after input voltage is removed before taking off cover.

TWO-YEAR WARRANTY

Power-One, Inc. will repair any power supply of its manufacture that does not perform to published specifications as a result of defective materials or workmanship for a period of 2 years from date of original purchase. No other obligations or liabilities are implied or expressed. Returns must be freight prepaid.

HOLDSWORTH & CO.
Sales Engineer
Box 298, Newtown Square, PA 19073
215-356-8550

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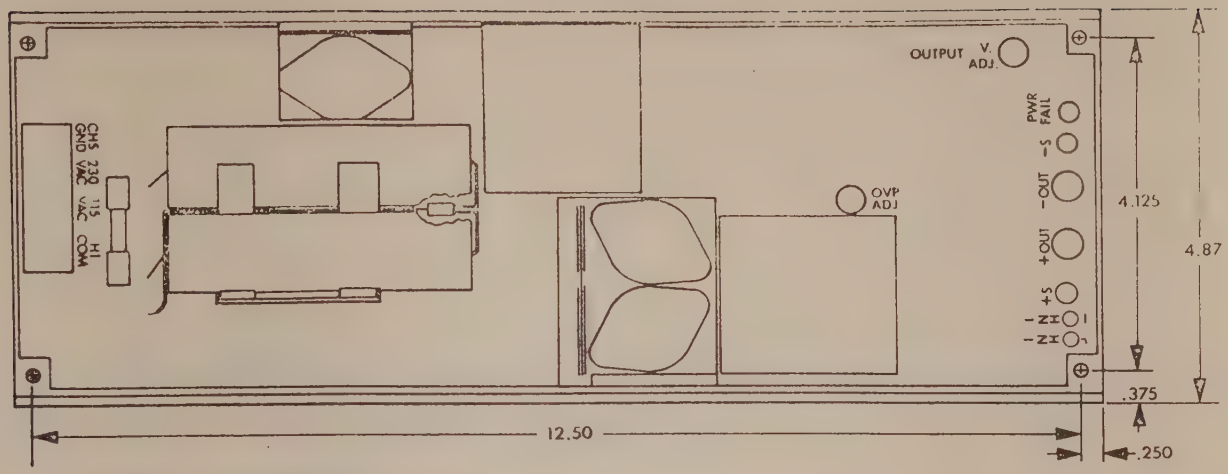
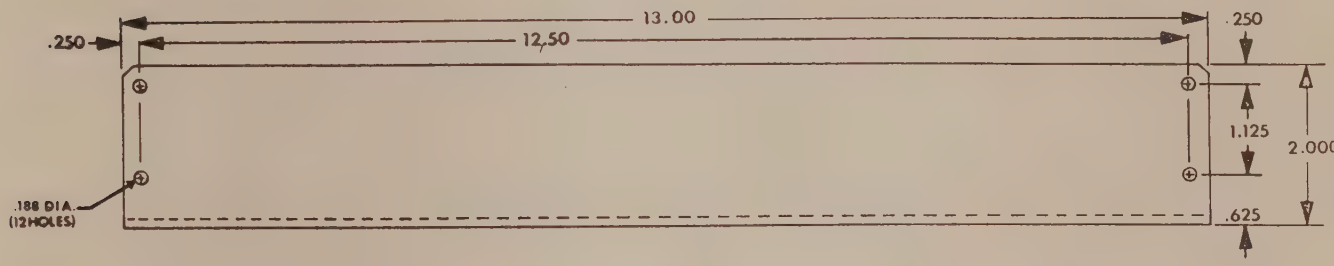
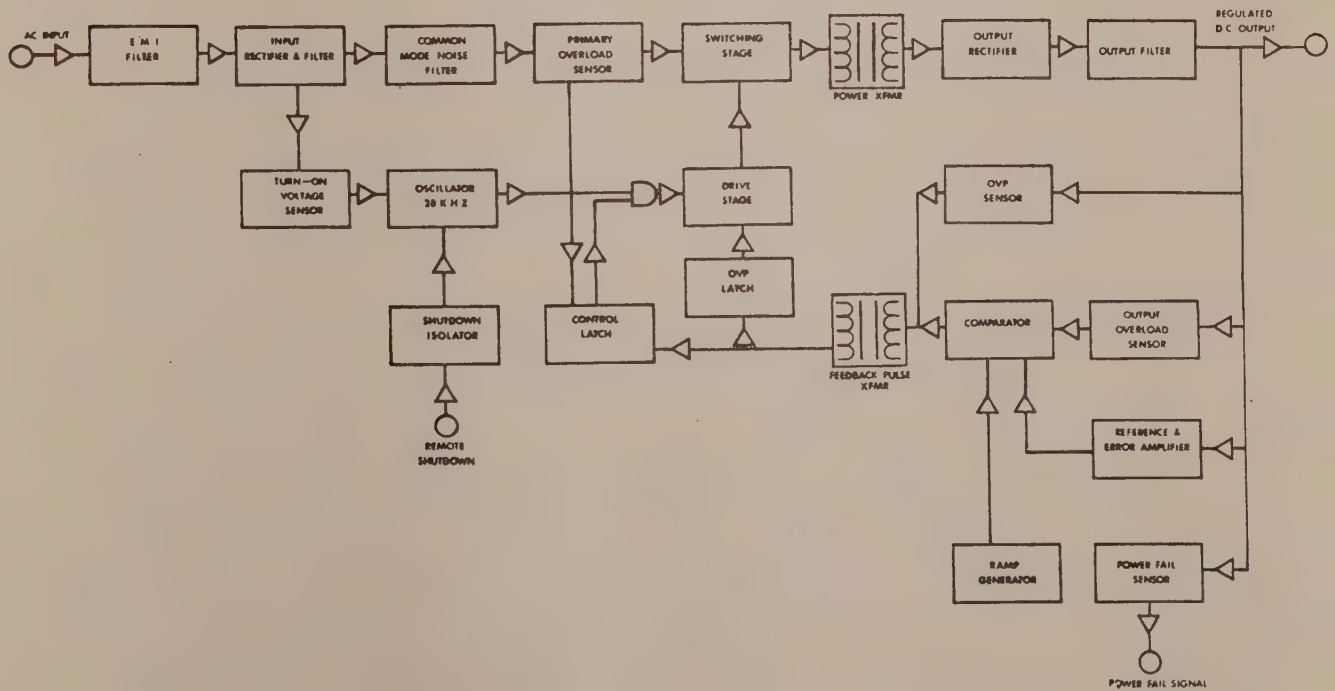


*COVER NOT SHOWN FOR CLARITY





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APPENDIX B

CRT DISPLAY MONITOR

B-1 GENERAL

This Appendix consists of a reproduction of the service manual for the CRT Display Monitor. The Model 607 DTTS uses Chassis Model 900946-1 (TTL), and Board Z49 for CRT display. This appendix can be used as an aid in understanding and troubleshooting the CRT Display Monitor.

AUDIOTRONICS SERIES 946 CRT DISPLAY MONITORS

1. GENERAL INFORMATION

The Model 946 Series of data display monitors are precision instruments intended for incorporation into commercial data processing equipment

Model 900946-TTL

This basic unit accepts TTL level drive signals. Standard polarity requirements are positive (logic 1) video drive to produce white, positive horizontal drive, and negative (logic 0) vertical drive. Reversal of a single diode permits use of positive vertical drive. The timing chart details the pulse requirements for TTL input signals

Model 900946-C/V

This model accepts composite video signals, sync negative, in accordance with NTSC or industrial standards, 0.5 to 2.5 Upp. Internal 75 ohm termination is provided. The terminating resistor may be removed for high impedance bridging.

Both models require 12 VDC input at a nominal 1.0 ampere. Major circuitry is contained on a single plug-in cirucit board. An accessory plug-in video/sync processor module is added for the composite video version.

Standard units are recognized under UL Standard 478 and comply with all applicable DHEW regulations relative to X-radiation.

2. SPECIFICATIONS

CATHODE RAY TUBE:	5" diagonal dimension, 70° deflection, 10 kV nominal HV at zero beam current; P4 phosphor.
POWER INPUT:	12.0 VDC, ±0.12 V, 1.0 A nominal.
GEOMETRIC DISTORTION:	Limited to simple bowing errors, not exceeding 2.0% of active raster height.
LINEARITY:	No specific character may vary in width or height by more than 10% of any adjacent character, or by more than 10% of the average of all characters in any row or column.
SCANNING SIGNALS:	Horizontal: 15.25 to 16.25 kHz; Horizontal blanking: 10.5 uS minimum. Vertical: 48 to 62 Hz; Vertical blanking: 650 uS minimum.
OPERATIONAL ENVIRONMENT:	Temperature: 5 to 55°C ambient. Humidity: to 90%, non-condensing. Altitude: to 10,000 ft.
RESOLUTION:	650 lines at center at 30 fL light output on 20% white window signal. Bandwidth is within 3dB from 10 Hz to 15 MHz.
CONTROLS AND ADJUSTMENTS:	All necessary controls or adjustments, including contrast and brightness, are mounted on the circuit boards. Connections for attachment of external brightness and/or contrast controls are accessible on the interface connector. See service instructions for installing external controls.
INTERFACE CONNECTORS:	Connection to customer system is made through standard 10-pin edge connector.

3. SPECIAL COMPONENTS

These monitors contain parts and circuitry designed to meet critical performance and/or safety requirements. Parts identified on the schematic diagram and in the parts list by double asterisk (**) may be replaced only by identical AVDD part numbers. Other components must have identical characteristics and their location and lead dress must conform with the original.

4. COMPONENT IDENTIFICATION

Part numbers are screened on the top of the circuit boards and coincide with those shown on the schematic diagram. Please note that some numbers have been duplicated on the main circuit board and on the composite video accessory board. For example, a Q1, R1, or C1 can be found on both boards. Be sure to refer the number to the specific board being discussed.

5. EXTERNAL BRIGHTNESS CONTROL

To install an external brightness control:

1. Remove original control from the main chassis board.
2. Connect jumpers, as shown, to interface connector terminals 2, 3, and 4.
3. Wire external 100k control to connector.

6. EXTERNAL CONTRAST (OR VIDEO LEVEL) CONTROL

Model 900946-01 (TTL):

If an external video level control is required, a 500 ohm potentiometer may be installed directly at the terminal video output, connected as shown on the dotted lines. Lead length and capacitance should be minimal to prevent loss of resolution. The TTL video output must be capable of driving the control. The internal video gain control may be left in the circuit and pre-set as desired.

MODEL 900946-02 (Composite Video):

To install an external contrast control, the following modifications are required:

Board Z40: Remove original control, VR1. Change R13 from 1.2 k to 390 ohms. Add jumper to connect terminal 2 of PL1.
Board Z49: Add C1 and connect external 500 ohm control as shown. Keep lead length and capacitance low and observe lead dress.

7. CRT REPLACEMENT

Safety glasses and gloves should be worn when CRT's are being handled. Avoid rough handling and do not scratch or nick the glass. Be sure the monitor is disconnected from all power sources.

CAUTION: The glass seal in the center of the CRT base pins can be damaged by careless handling. Use care in removing or installing the socket. Breakage will void the CRT warranty.

The tube is removed or replaced from the front of the mainframe. Discharge the tube by shorting the anode button to ground. Remove the CRT socket and anode connector, and unplug the deflection yoke.

Loosen the two screws on the mounting band and lift tube and yoke out the front of the mainframe. Note the position of any tape placed between the tube and the band. Replace any tape that cannot be reused.

Transfer the yoke to the new tube and reinstall. The tube face must touch the positioning flanges on the band.

8. DEFLECTION YOKE INSTALLATION AND ADJUSTMENT

The yoke must be firmly clamped against the tube bell and the display properly centered before final adjustments can be made. Display a test pattern at normal contrast and brightness.

Because of slight electrical and mechanical differences between individual CRT's or yokes it is usually necessary to correct geometric distortion. During original factory setup auxiliary magnets were cemented to the yoke to match it with its CRT. When either a yoke or CRT are changed it may be necessary to add or adjust correction magnets.

9. CIRCUIT BOARD REMOVAL

Be sure that all power is disconnected. Remove the interface connector from the rear of the chassis board. Discharge the CRT and remove the anode connector. Unplug the yoke and the CRT socket.

Remove the single screw at the lower left corner, below the CRT, on the front of the mainframe. The board assembly will now slide out the rear.

10. POWER SEMICONDUCTOR REPLACEMENT

Damper diode D5 and horizontal output transistor Q4 are power devices mounted on the heat sink on the cirucit board. In replacing these components heat sink compound must be applied and mounting screws secure in order to assure efficient heat transfer. D5 requires no insulation, but Q4 must be insulated from the sink. Replace all washers, spacers, or insulators exactly as found on the original.

11. VIDEO LINE TERMINATION

On Model 900946-02, the composite video input is terminated by a 75 ohm resistor (R 1). If a number of monitors are fed from a single video source R1 may be removed for high impedance bridging. It is essential that a single monitor, or the last unit in a looped-through group, be properly terminated.

12. SETUP ADJUSTMENTS

Brightness and Contrast:

With a dim test pattern displayed on the screen, adjust brightness to just extinguish the background. Contrast (or video gain) is then advanced to produce a normal display. Excessive brightness or contrast will cause a loss of display detail. If external controls have been provided, be sure that the operator has been instructed in their use.

Vertical Frequency:

Turn the vertical frequency control until the pattern rolls slowly down, then return to the point at which it again locks in. Continue rotation for about another ten degrees for maximum stability.

Horizontal Frequency:

Rotate the horizontal frequency control and notice the range over which it locks in. Set the control to the center of its lock-in range. The control may be shifted slightly to center the display on the raster.

For very precise adjustment of frequency, connect a jumper between circuit ground and the junction of R2/R3. This disables sync and the oscillator will free-run. Adjust the frequency control for minimum horizontal motion of the display. When the jumper is removed the oscillator will be locked in at the optimum control setting. With this adjustment, if the display is not properly centered on the raster, consult with your dealer for modification of horizontal oscillator timing.

Display Size and Linearity:

These monitors have been factory-adjusted for a most popular CRT display size. If desired, height and width may be changed slightly without affecting linearity. The linearity controls ordinarily do not require change from the factory setting unless components have been replaced.

The width control is adjusted with a standard hexagonal plastic alignment tool. Horizontal linearity adjusts by turning the cylindrical magnet on the base of the coil. A small screwdriver may be used, but it is best to use a plastic tool which fits the socket hole of the magnet.

Vertical and horizontal linearity controls also affect display size. Linearity must be correct before final adjustment of height, width, or centering.

Focus:

Focus is best adjusted on a full screen of characters displayed at normal contrast and brightness. Adjust focus for the best compromise in detail over the entire display.

13. TROUBLE SHOOTING HINTS

Before any other tests, be sure that the power input voltage and the input signals are present and within tolerance. Voltages should be measured with a digital meter and a probe having an isolation resistor of at least 100 kilohms. High voltage must be checked by meter and the proper HV accessory probe. Do not arc high voltage to ground.

Do not attempt to measure DC voltage at any point on the flyback transformer where high pulse voltages are present. Rectified pulse voltages may be measured on the filtered side of the diode. Pulse amplitudes anywhere in the circuitry must be checked by oscilloscope and low-capacitance probe.

The monitor circuitry can be broken down into a few fundamental functions: video processing, vertical deflection and horizontal deflection. Trouble symptoms will indicate the area in which a malfunction occurs. Most faults can be located by signal tracing through the circuit with the oscilloscope and by measurement of the various supply voltages.

14. COMPARISON OF TTL AND COMPOSITE VIDEO CIRCUITRY

The basic circuits found on the main chassis board (Z49/182080) are used for both TTL and composite video input signals. The video output, vertical oscillator, and horizontal processor obtain their drives from individual TTL signals.

For composite video signal processing, S01 is added to the Z49 board to mate with a plug-in module (Z40/181072). This accessory board contains additional video amplifiers, contrast control provisions, and the sync processor which derives the deflection drive pulses from the composite signals.

15. VIDEO PROCESSOR MODULE Z40/181072

The composite video signal received through Pin 3 or PL1 feeds a complementary feedback amplifier Q3/Q4. The emitter output of Q3 supplies the low-Z drive for the contrast control and the following amplifier. Feedback through C5/R12 adjusts the amplifier response for best driving of the sync amplifier and separator Q5. The RC network feeding the base of Q5 is optimized for sync pulse shaping.

The output of Q5 contains only positive sync information, with the video removed by clipping action. C8 differentiates the signal to form the horizontal sync pulses fed to Q1 on the main chassis board. Vertical sync is integrated through R17 and the following RC network on the main chassis.

Contrast control VR1 (or an external contrast control) adjusts the level of signal fed to wide-band amplifier Q1/Q2. The output of this amplifier, through Pin 8 of PL1, drives the video output stage.

16. VIDEO OUTPUT STAGE

The video output stage Q2 receives its drive either directly from the TTL pulses or from video processor board Z40. Diodes D1/D2 provide DC restoration by clamping black level. They also supply temperature-compensated bias voltage for Q2. The video gain control in Q2 emitter circuit is used on the TTL version. The fixed RC network is substituted on the composite video models. In either case, the network is designed to provide high frequency phase compensation.

A positive pulse causes Q2 collector current to draw the cathode of the CRT in a negative direction, increasing beam current and brightening the screen. L1 provides high-frequency peaking.

D3/C23 act to limit beam current to prevent overdrive of the CRT. If the tube is driven to excessive brightness its cathode current causes it to become self-biased by the voltage drop across C23. This effectively limits CRT beam current. Overdrive will cause deterioration of display quality because of compression or clipping of white and black.

17. RETRACE BLANKING

Blanking amplifier Q5 receives positive pulses derived from the horizontal and vertical deflection circuits and shaped by the networks feeding its base. These signals are amplified and inverted by Q5 and applied to G1 of the CRT to black out the screen during retrace periods. ZD1 clamps the positive excursion of the blanking voltage to prevent errors due to a change in the video supply voltage.

18. VERTICAL DEFLECTION

Integrated circuit IC1 performs the functions of vertical oscillator, driver, and output stages. The RC time constant of VR2/R43/C30 establishes the vertical frequency. In the absence of sync the oscillator will free-run to maintain sweep. Synchronization is accomplished by applying pulses of either polarity to Pin 8 through the shaping network C31/C32/R42. Diode D8 prevents false triggering and must be connected with its cathode grounded for negative sync input, or reversed if positive sync is used.

A sawtooth ramp generated across C16, C17, appears as the buffered output of Pin 1. Amplitude of the sawtooth is controlled by the resistive loading on Pin 7. Height is adjusted by varying VR4. The Pin 1 output is level-shifted internally to provide drive for the output stages, which drive the deflection yoke through Pin 4.

A portion of the Pin 1 output is fed back through R20/VR3 for adjusting display linearity. R25 couples the ramp voltage to the input of the driver stages. The RC networks in the output circuits provide yoke damping and additional feedback for stability. Diode D9 acts as a retrace boost to shorten vertical retrace time. The pulse appearing at Pin 3 is used for vertical retrace blanking.

19. HORIZONTAL DEFLECTION

Integrated circuit IC2 is a horizontal processor containing a voltage-controlled oscillator, phase detector, and pre-driver section. The oscillator is an RC type, with timing controlled at Pin 7. An internal regulator maintains a stable reference voltage at Pin 6.

The incoming horizontal drive or sync pulse is amplified and inverted by Q1 and applied as a negative sync to Pin 3. This signal is compared in phase with a sawtooth reference voltage at Pin 4. The phase detector output at Pin 5 is coupled to the oscillator through R6. Any phase difference between sync and reference will cause current to flow to correct oscillator phase. The sawtooth reference is derived from the horizontal retrace pulse and shaped by the RC network on Pin 4.

In accordance with DHEW requirements, ZD2 and D11 act as a safety circuit to prevent operation of the monitor with excessive input voltage. D11 is placed in series with ZD2 to compensate for the zener capacity. If a failure in the regulator circuit of the external power supply causes the nominal 12 VDC to rise to about 16 V, ZD2 will conduct and raise the frequency of the oscillator beyond the lock-in range of the frequency controls. A further increase may cause the oscillator to shut down completely. Continued application of excessive DC input may cause thermal runaway and other destructive malfunctions.

The oscillator output is shaped by a pre-driver section to produce a pulse of the proper duty cycle for feeding driver transistor Q3. Driver transformer T1 is phased so that Q4 is turned off when Q3 conducts, initiating horizontal retrace. Q4 drives a conventional flyback high voltage system. The high reactive voltages which appear at the different transformer taps are rectified to supply DC for the CRT and the video amplifier.

Width control L2 contains both series and shunt windings, permitting width adjustment without affecting flyback tuning. Linearity control L3 is a saturable reactor whose inductance varies with yoke current. The rotatable magnet on the coil base permits precise adjustment of the display.

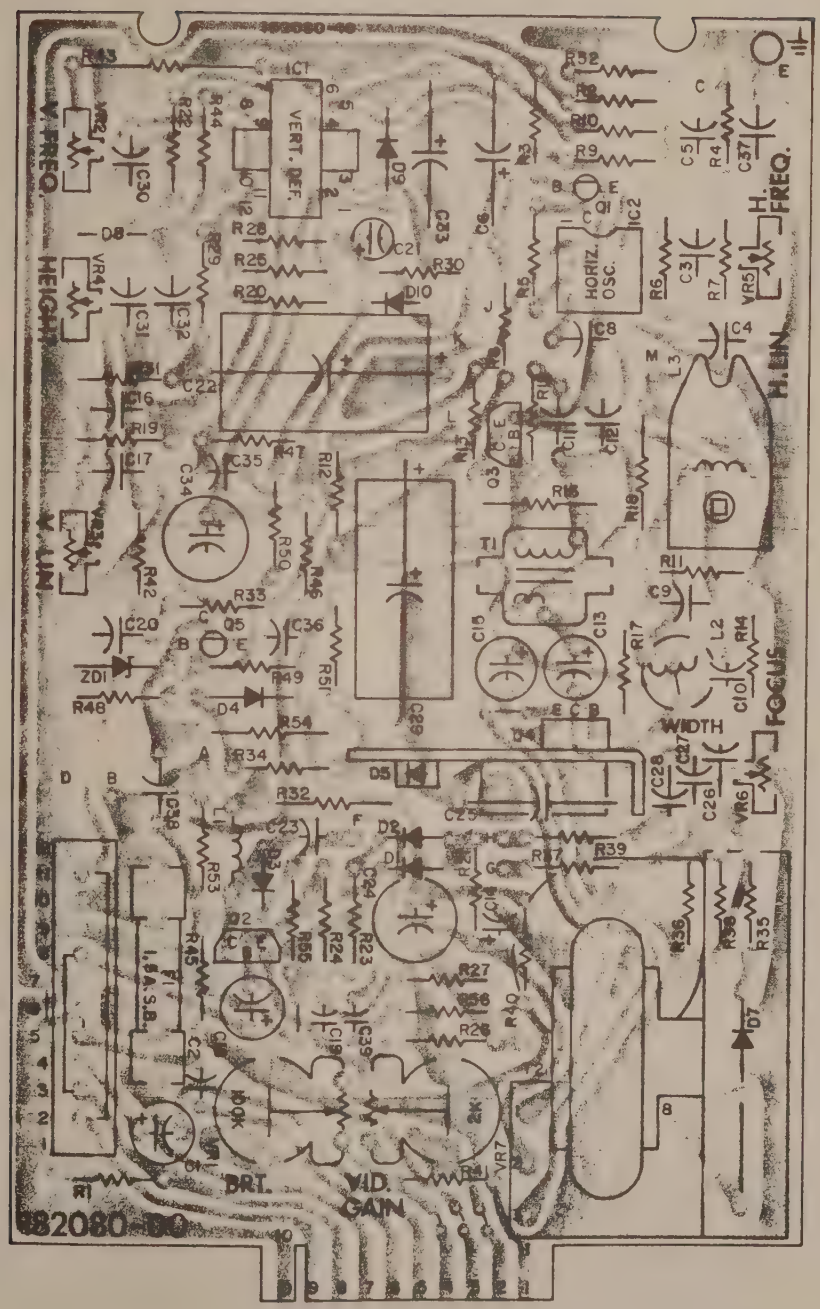
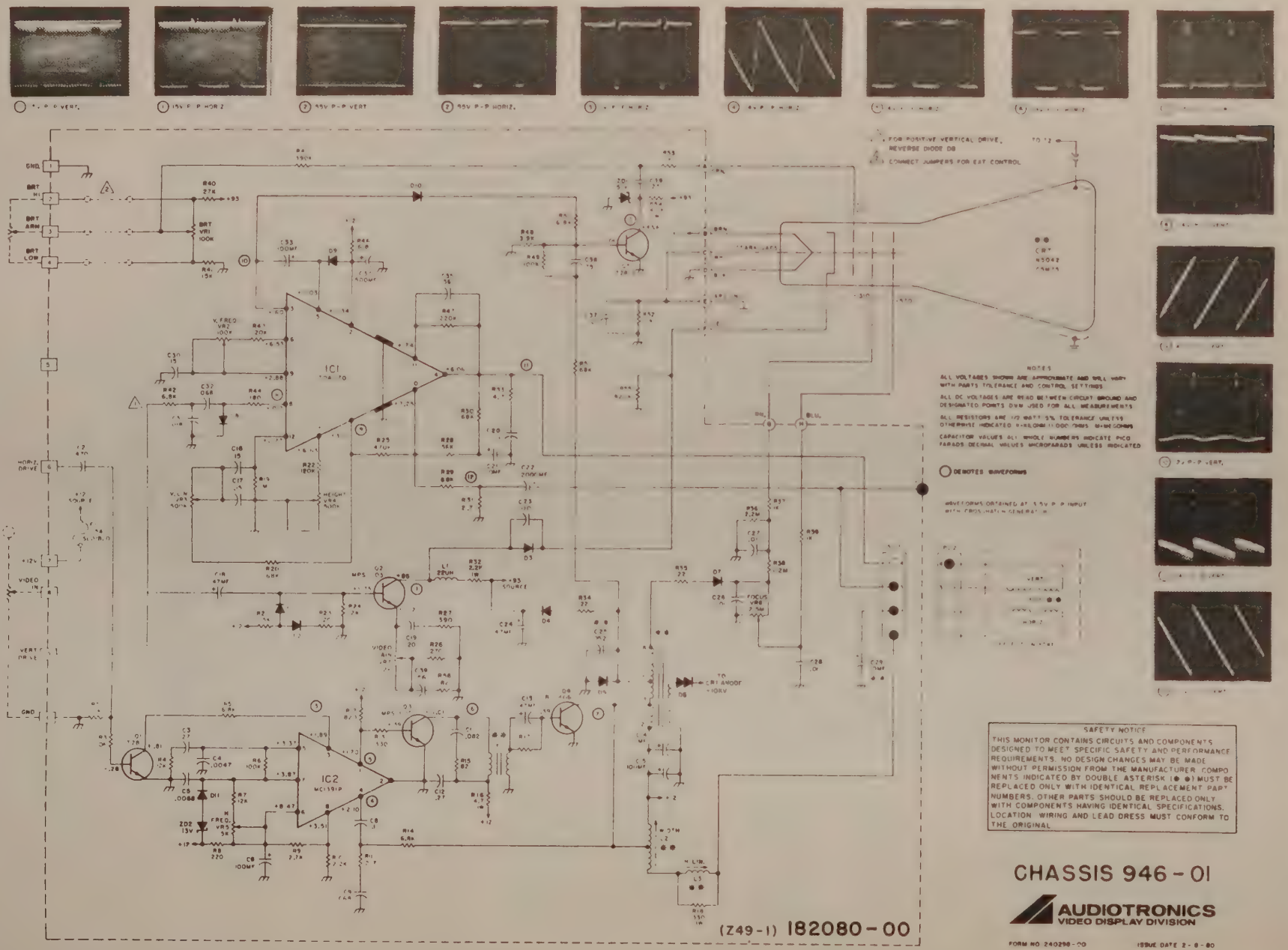

V. FREQ.
HEIGHT
V. LIN.
VERT. DEF.
HORIZ. OSC.
H. FREQ.
H. LIN.
WIDTH
FOCUS
BRT.
VID. GAIN
082080-00

FIGURE 3

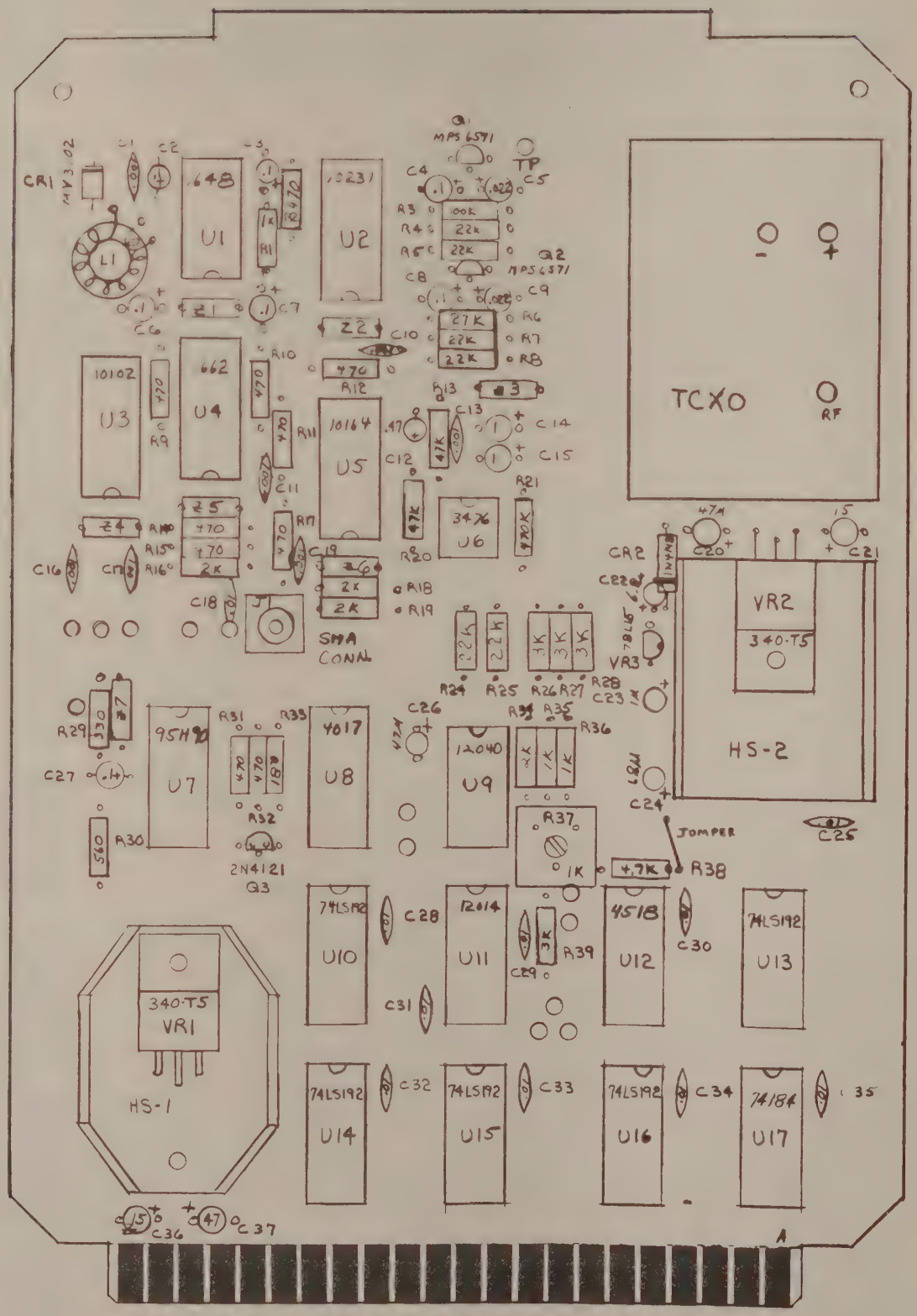

SAFETY NOTICE
THIS MONITOR CONTAINS CIRCUITS AND COMPONENTS DESIGNED TO MEET SPECIFIC SAFETY AND PERFORMANCE REQUIREMENTS. NO DESIGN CHANGES MAY BE MADE WITHOUT PERMISSION FROM THE MANUFACTURER. COMPONENTS INDICATED BY DOUBLE ASTERISK (**) MUST BE REPLACED ONLY WITH IDENTICAL REPLACEMENT PART NUMBERS. OTHER PARTS SHOULD BE REPLACED ONLY WITH COMPONENTS HAVING IDENTICAL SPECIFICATIONS. LOCATION, WIRING AND LEAD DRESS MUST CONFORM TO THE ORIGINAL.
CHASSIS 946 - 01
AUDIOTRONICS
VIDEO DISPLAY DIVISION
FORM NO. 240298 - 00
ISSUE DATE 2 - 8 - 80
(Z49-1) 182080-00

APPENDIX C

FREQUENCY SYNTHESIZER MODULE

C-1 GENERAL

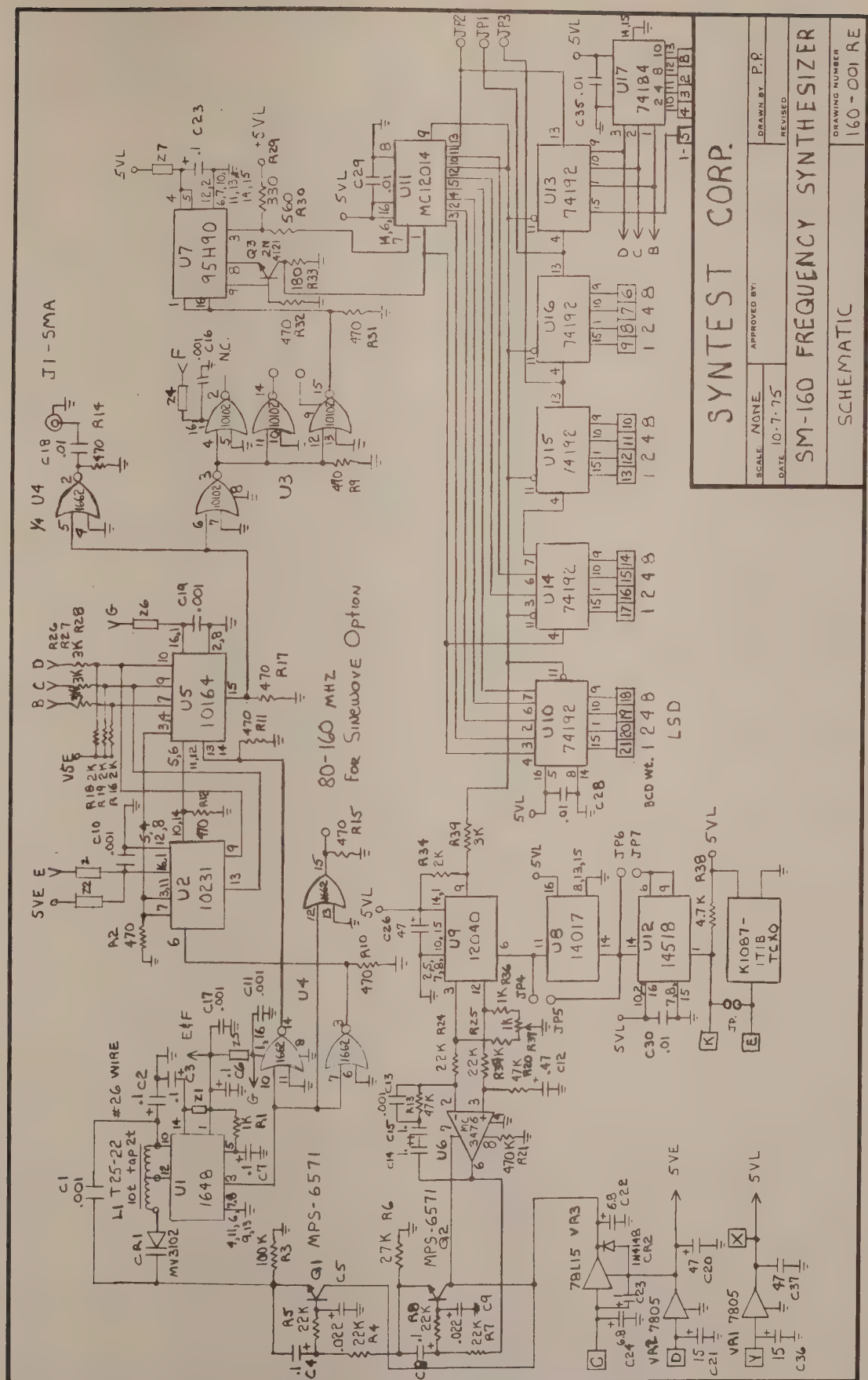
This appendix is a reproduction of the data sheet for the Frequency Synthesizer Module, SM-160, used in the Model 607 DTTS. The appendix also includes a Parts List of the module. This appendix can be used to aid in understanding and troubleshooting the SM-160 module.



SYNTEST CORP

ASSEMBLY SM 160

160-002 REV E


SYNTEST CORP.
SCALE: NONE
DATE: 10-7-75
APPROVED BY:
DRAWN BY P.P.
REVISED
SM-160 FREQUENCY SYNTHESIZER
SCHEMATIC
DRAWING NUMBER 160-001 RE
80-160 MHZ FOR SINEWAVE OPTION
J1-SMA
U1 1648
U2 10231
U5 10164
U7 95H90
U11 MC12014
U13 74192
U14 74192
U15 74192
U16 74192
U17 74184
U9 12040
U8 14017
U12 14518
K1087-1T1B TCXO
U6 MC3476
Q1 MPS-6571
Q2 MPS-6571
L1 T25-22 10t tap 2t
#26 WIRE
LSD
BCD Wt. 1248
1248
5VL
5VE
JP1
JP2
JP3
JP4
JP5
JP6
JP7
VR1 7805
VR2 7805
VR3 78L15
1N4148

REFERENCE DES.	QUA.	PART NO.	DESCRIPTION
R1,35,36	3	1K	RES. 1/4 WATT 5%
R2,9-12,14,15			
R17,31,32	10	470 OHM	RES. 1/4 WATT 5%
R3	1	100K	RES. 1/4 WATT 5%
R4,5,7,8,24,25	6	22K	RES. 1/4 WATT 5%
R6	1	27K	RES. 1/4 WATT 5%
R13,20	2	47K	RES. 1/4 WATT 5%
R16,18,18,34	4	2K	RES. 1/4 WATT 5%
R21	1	470K	RES. 1/4 WATT 5%
R26-28,39	4	3K	RES. 1/4 WATT 5%
R29	1	330 OHM	RES. 1/4 WATT 5%
R30	1	560 OHM	RES. 1/4 WATT 5%
R33	1	180 OHM	RES. 1/4 WATT 5%
R38	1	4.7K	RES. 1/4 WATT 5%
R37	1	1K	POT. (840M-1K) (72PMR-)
C1,10,11,13,16			
C17,19	7	.001uf	CAPACITOR 100V
C2-4,6-8,27	7	.1uf	CAPACITOR 35V TAG
C5,9	2	.022uf	CAPACITOR 100V
C12	1	.47uf	CAPACITOR 35V TAG
C14,15,23	3	1uf	CAPACITOR 35V TAG
C18,25,28-35	10	.01uf	CAPACITOR 100V
C20,26,37	3	47uf	CAPACITOR 6.3V TAG
C21,36	2	15uf	CAPACITOR 20V TAG
C22,24	2	6.8uf	CAPACITOR 35V TAG
CR1	1	MV3102	DIODE
CR2	1	1N4148	DIODE
J1	1	142-0298-001	CONN. (E.F. JOHNSON)
L1	1	S-102	COIL ASS'Y
VR1,2	2	LM340T-5	REGULATOR (MC7805CT)
VR3	1	78L15	REGULATOR
HS-1	1	6106B-14	HEAT SINK THERMALOY
HS-2	1	LAD66A4CB	HEAT SINK IERC
Q1,2	2	MPS6571	TRANSISTOR
Q3	1	2N4121	TRANSISTOR
Z1-7	7	S-108	H/L FREQ. FER. ASS'Y
U1	1	MC1648P	I.C.
U2	1	MC10231P	I.C.
U3	1	MC10102P	I.C.
U4	1	MC1662P	I.C.

REFERENCE DES.	QUA.	PART NO.	DESCRIPTION
U5	1	MC10164P	I.C.
U6	1	MC3476P1	I.C.
U7	1	95H90DC	I.C.
U8	1	4017	I.C.
U9	1	MC12040P	I.C.
U10,13-16	5	74LS192	I.C.
U11	1	MC12014P	I.C.
U12	1	MC14518BCP	I.C.
U17	1	74184	I.C.
TCXO	1	T30-12	TCXO-ISOTEMP
	1	C850801	8 PIN SOCKET
	2	C851401	14 PIN SOCKET
	14	C851601	16 PIN SOCKET
	1	160-002	P.C. BOARD
	2	CBE-11	EXTRACTOR
	1	TP-3-22-1-S-01	CONNECTOR TEKA

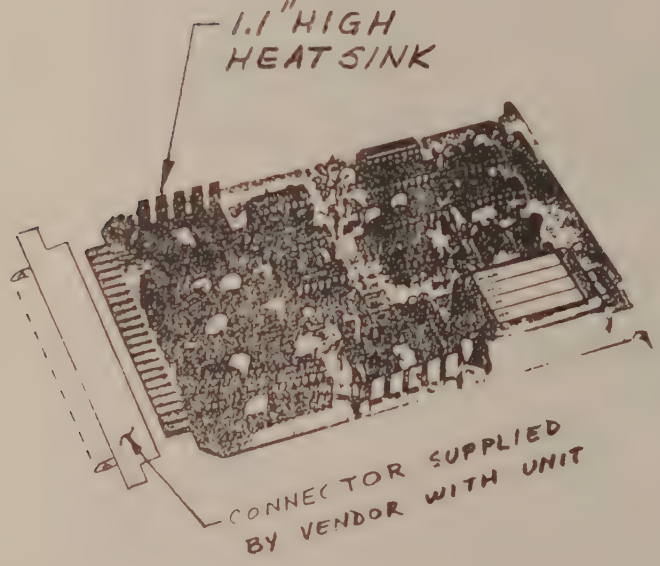
syntest CORPORATION

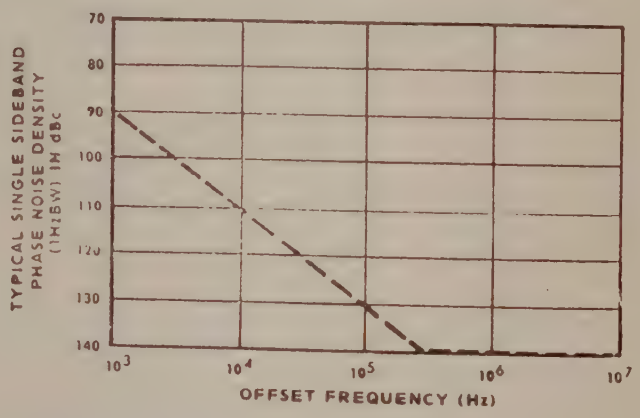
DATA SHEET

SM-160

Frequency Synthesizer Module

The SYNTEST SM-160 is an advanced 5 digit modular synthesizer employing a single phase locked loop to provide high performance over a wide range at very low cost. Designed as a systems component, the SM-160 provides 20MHz to 160MHz ECL signals into a 50Ω load with low phase noise and spurious signals. Fast programming makes the SM-160 even more attractive for the systems user. Extensive testing and high margin design practices guarantee high reliability for systems applications.





Compact Solid State Design

Output Frequency 20MHz to 159.999MHz

Very High Performance to Price Ratio

Frequency Digitally Selectable by BCD TTL Lines

High Stability Internal Oscillator, ($\pm 1 \times 10^{-6}$) over 0 – 50°C

Spurious Outputs 60dB below Full Output

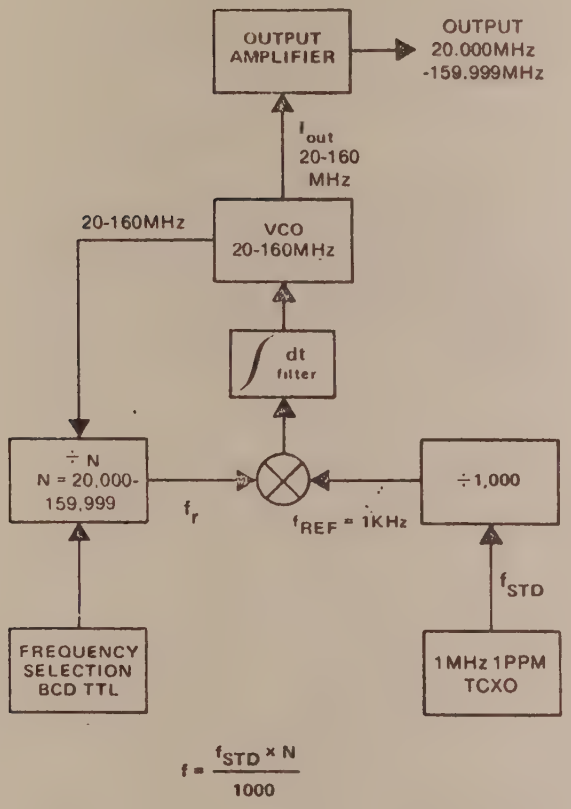
Custom Configurations Available

Typical Applications

- Provide stable, low phase noise source to stabilize microwave oscillators
- Use in plotting and alignment of active and passive filters
- Inexpensive variable frequency generator in automatic test sets using BCD programming
- Provide rapid inspection and testing of large array comb filters
- Calibration standard for analog oscillators
- Precision variable clock for I.C. system testing
- Receiver oscillator
- Variable R.F. source for N.M.R.

142-058-□
SHEET 2

Basic Block Diagram



The Model SM-160 Frequency Synthesizer Module uses a single phase-locked loop to provide wide operating range at low cost. Update rate is 1KHz providing 1KHz steps at all operating frequencies from 20MHz to 160MHz. Use of monolithic regulators on board provides excellent isolation from external variables.

Pin connections are:

	MSD	2nd MSD	3rd MSD	4th MSD
Function	1	8 4 2 1	8 4 2 1	8 4 2 1
Pin Number	B	2 3 4 5	6 7 8 9	10 11 12 13
Digit	x 100MHz	x 10MHz	MHz	x100KHz

	5th MSD	LSD	VOLTAGES
Function	8 4 2 1	8 4 2 1	+24V +10V +5VL output
Pin Number	14 15 16 17	18 19 20 21	C D,Y X
Digit	x 10KHz	KHz	

GND: 1, 22, A, E-W, Z
OUTPUT: SMA FEMALE,

Specifications

FREQUENCY RANGE:	20.000 to 159.999MHz (Five Digits with 60% Overrange)
FREQUENCY RESOLUTION:	1000Hz from 20.160MHz
FREQUENCY SELECTION:	5½ Digit BCD (frequency) (1, 2, 4, 8 BCD) All Programming Lines are TTL Positive True.
FREQUENCY ACCURACY AND STABILITY:	±1PPM from 0 to 50°C Internal TCXO
OUTPUT LEVEL:	ECL Levels into 50Ω 0.7 Volts P.P. into 50Ω +2dBM ±1dB
OUTPUT WAVEFORM:	Squarewave Rise Time – 2.5ns typical Fall Time – 2.5ns typical Output Connector: SMA
NON-HARMONIC SPURIOUS OUTPUT:	60dB below Full Output
SIGNAL-TO-PHASE NOISE RATIO:	30dB below 1 radian (Measured in a band of 30KHz excluding a 10Hz notch centered on the output frequency)
SETTLING TIME:	10 milliseconds to within 10% of Step
OPERATING TEMPERATURE:	Operating 0 to 50° C Storage -20 to +72° C
POWER REQUIREMENTS:	+8 to +10VDC at 0.8A +22 to +30VDC at 50ma
DIMENSIONS:	Length: 6.5" (165mm) Height: 1.1" (28 mm) Width: 4.5" (114mm)
CIRCUITRY:	All Solid State, CMOS, ECL, and TTL with Monolithic Regulators
MATING CONNECTOR:	TRW Cinch 50 44A 30 OR EQUAL Connector is 44 pin .156 ctrs
SHIPPING WEIGHT:	1.5 lbs (.68Kg)

Your Representative –

syntest CORPORATION
169 Millham Street • Marlboro, Mass. U.S.A. 01752
Telephone (617) 481-7827 TWX 710 390 7659

142-058-LJ SHEET 3

Printed in U.S.A.

APPENDIX D

FRONT PANEL KEYBOARD

D-1 GENERAL

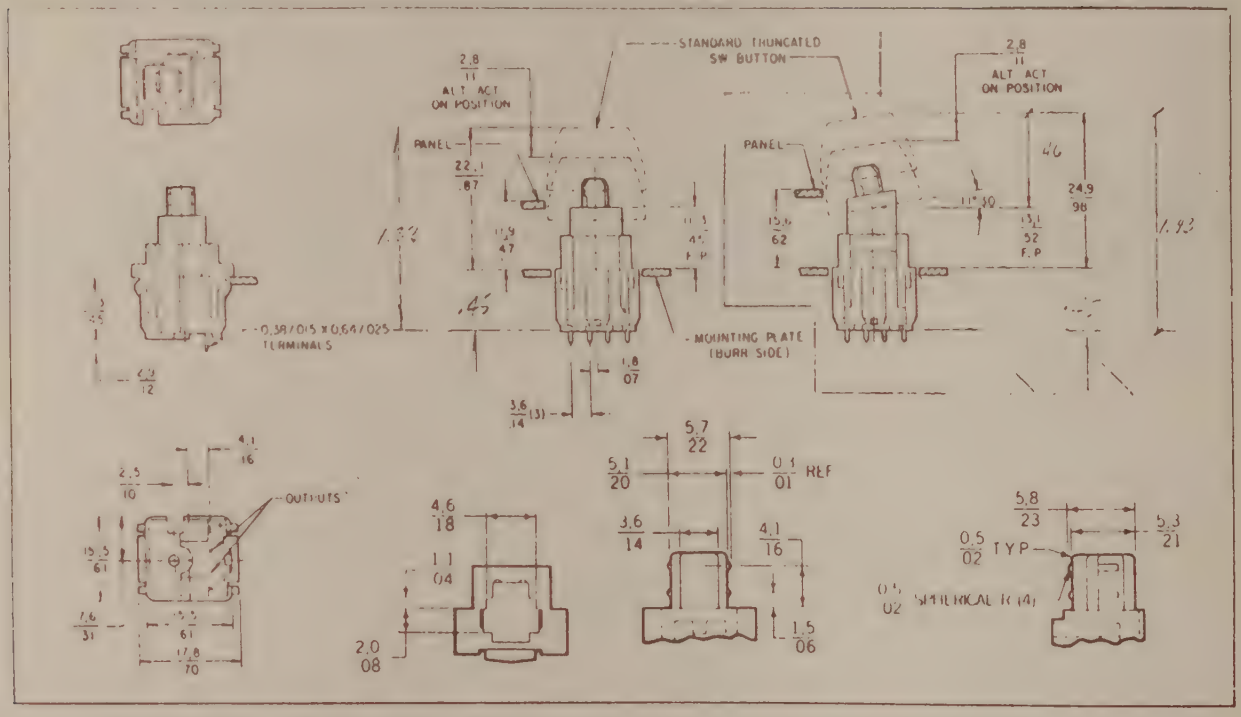
This appendix is a reproduction of the product sheet for the SD Switch Module used on the front panel keyboard; the assembly drawing for the front panel keyboard is shown in Section 6. The specification numbers for the SD Switch Module used in the Model 607 DTTS are 107-166-004, -005, and -006. This appendix can be used to aid in understanding and troubleshooting the front panel keyboard.

Low profile solid state switch module

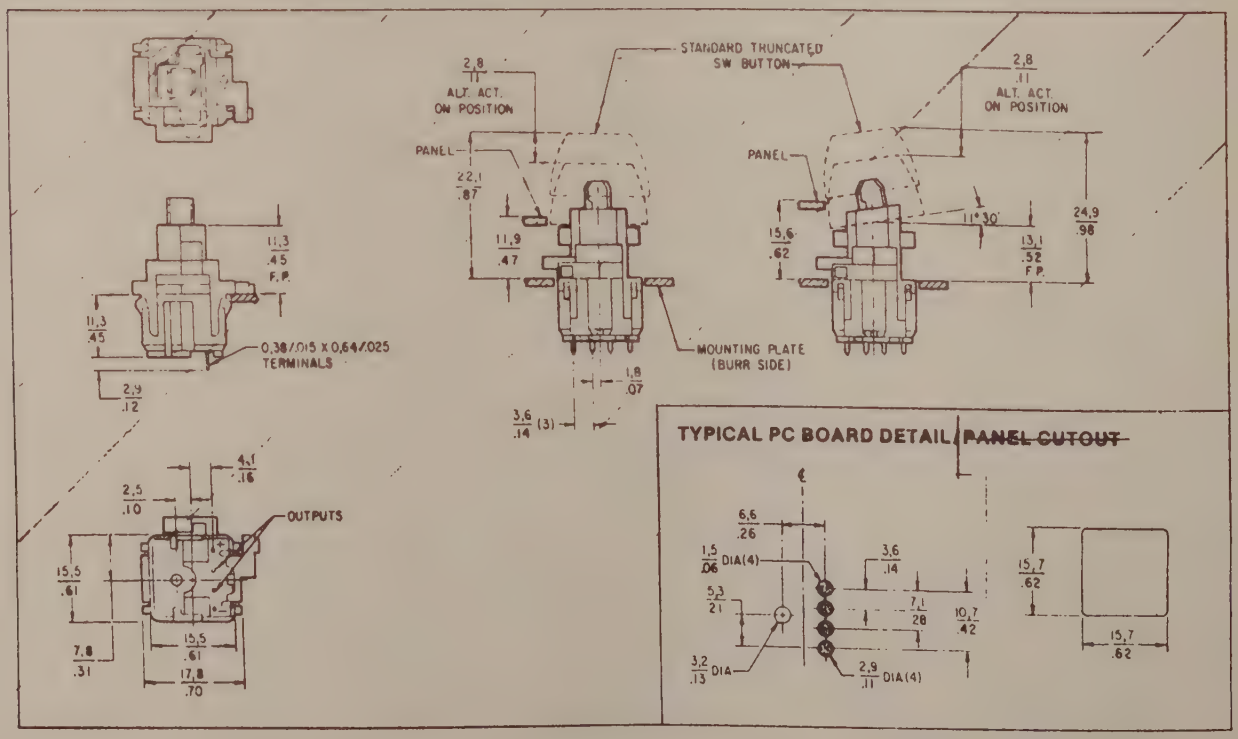
-004	-005	-006

MOUNTING DIMENSIONS STANDARD SD MODULE (For reference only)

(Level, Pulse, Logic Scan)



MOUNTING DIMENSIONS (Secretary Shift Mechanism)



107-166-□
SHEET 5

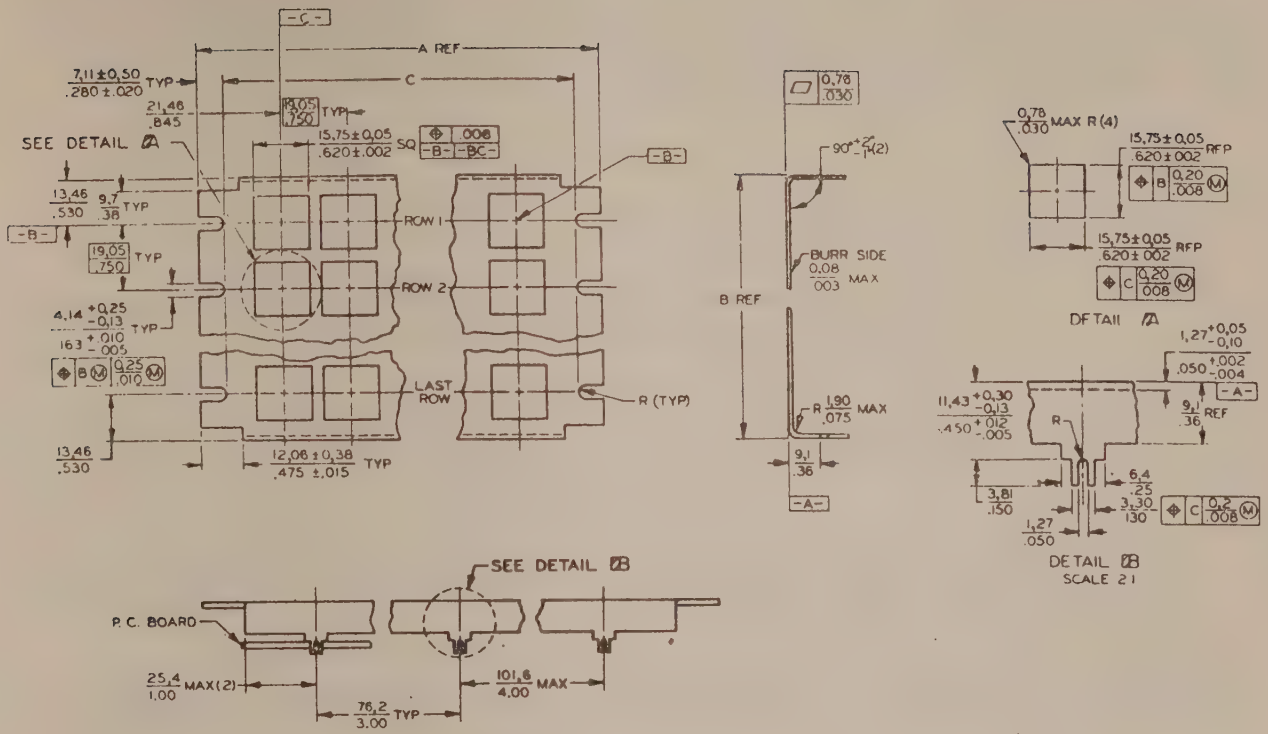


Figure 2
SD Mounting Panel Dimensions

The spread tabs are spread using a suitable tool such as a screwdriver as shown in Figure 3 to firmly attach the panel to the PC board.

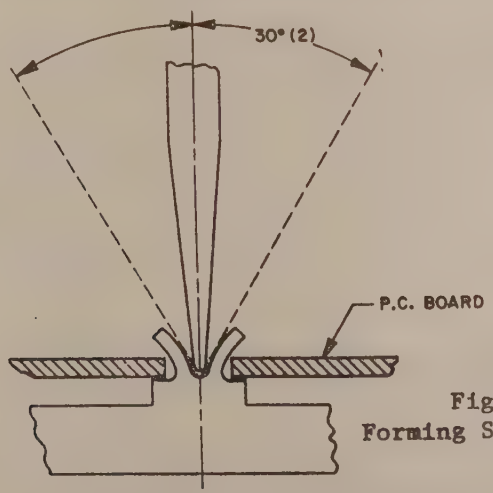


Figure 3
Forming SD Spread Tab

107-166-□
SHEET 7

The locations of the spread tabs are dictated by the specific panel and printed circuit board application. Spread tab locations must correspond to the spread tab holes in the PC Board which in turn relate to the switch terminal holes in the PC board. General recommendations for spread tab location are as follows:

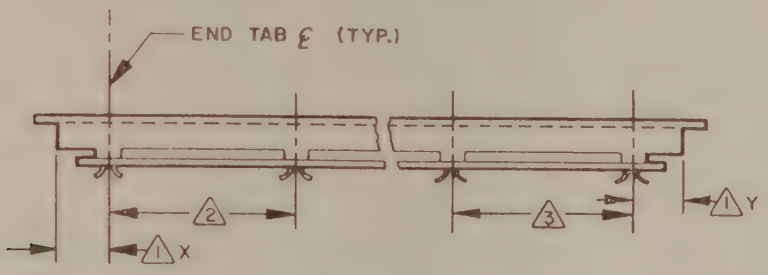


Figure 4
General Spread Tab Location

1. The center line of the panel and tabs should be located less than 1.0 inch from the end of the panel form. Dimension (X) should equal dimension (Y). See Figure 4, dimension 1.

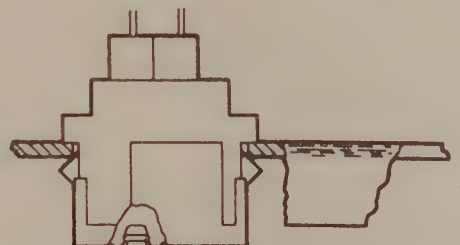
2. The intermediate tabs should be placed 3.0 inches on center referenced from the end tab. See Figure 4, dimension 2.

3. Additional tabs are required if the distance between the last intermediate tab and the opposite end tab is greater than 4.0 inches. See Figure 4, dimension 3.

4. The spread tabs should be placed symmetrically along the front and back edges of the panel.

MICRO SWITCH uses plastic retainer pins (catalog listing SD-10381) to provide support to the printed circuit board during wave soldering, handling and use. These pins assemble through the PC board to the module housing as illustrated in Figure 5.

Note: A .125 dia. hole is required in the PC board for each retainer pin used (see Fig. 6 for hole location).



-007

Figure 5
Retainer Pin Assembly

NOTE: USE SCREW P/N 127-104-003 WITH WASHERS P/N 128-200-802 & 128-202-134 WHEN THE MANUFACTURED PANEL (CHASSIS) IS NOT USED.

107-166-□ REV B
SHEET 8

A retainer pin is recommended in a module under the following conditions:

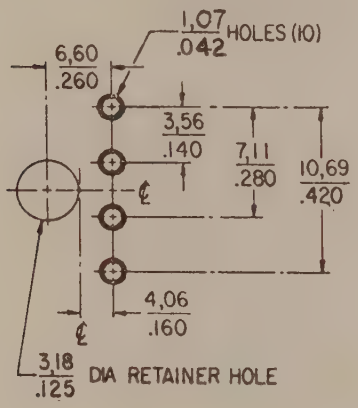
1. Row end modules in the center row of a 5 row keyboard. An additional retainer pin should be added for every additional two rows of modules.
   Example: a 5 row keyboard - add one retainer pin in each end module of the center row.
   A 7 row keyboard - add one retainer pin in each end module of rows 3 and 5.

2. The retainer pins should be located in the appropriate rows and spaced not less than 2 inches or greater than 4 inches apart throughout the rows.

PC BOARD RECOMMENDATIONS

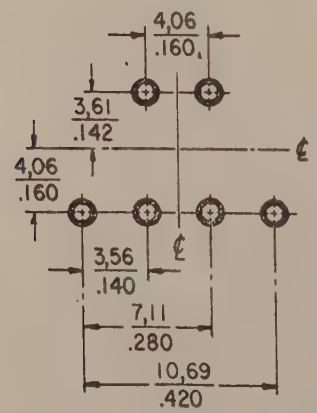
Material: .062 thick.

Recommended hole sizes and locations for the switch modules are shown in Figure 6. Good design practice should be used for pad sizes as well as conducting paths. See Figure 7 for the recommended hole for spread tabs.



TOLERANCES				
APPLY TO DESIGN UNITS. CONVERSIONS ARE ONLY FOR REFERENCE. UNLESS NOTED, TOLERANCES ARE ±				
	DIM. & mm	TOL. mm/in	DIM. in	TOL. mm/in
NO PLACES	X	1/.04		
ONE PLACE	X,X	0,4/.016	X.X	0,8/.03
TWO PLACES	X,XX	0,15/.006	X.XX	0,38/.015
THREE PLACES			X.XXX	0,13/.005
ANGLES				
DESIGN UNITS	SI METRIC ☐		US CUSTOMARY ☐	
RAW MATERIAL—COMMERCIAL STANDARD MICRO SWITCH STANDARDS APPLY				
DIMENSIONS ARE TO BE MET BEFORE PROTECTIVE COATINGS ARE APPLIED				

Figure 6
Hole Size and Location



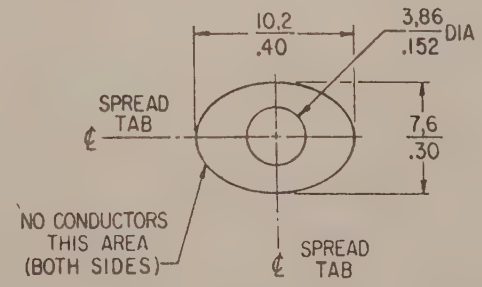


Figure 7
Spread Tab Hole Size

107-166-☐ REV E
SHEET 9

Figure 8 illustrates a typical PC board and the recommended dimensions and tolerances.

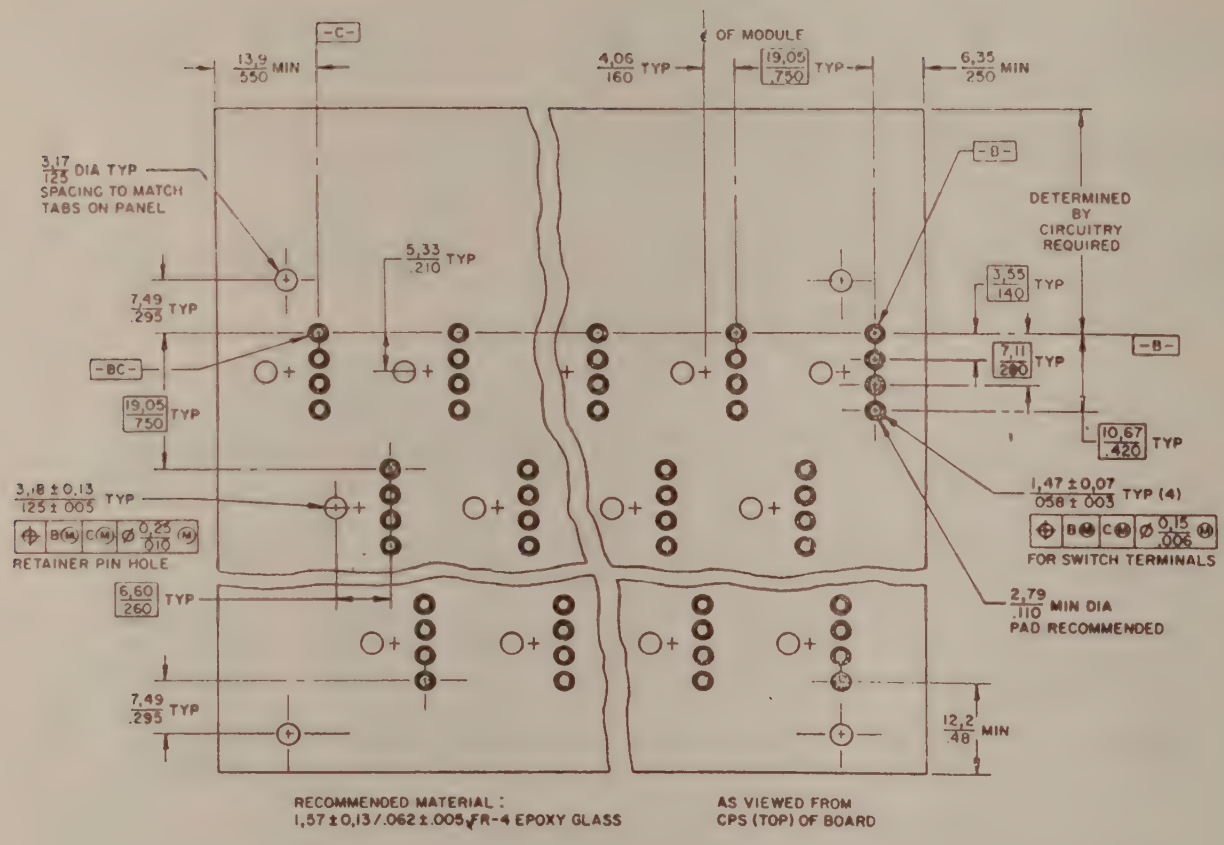


Figure 8
Typical PC Board

SD ASSEMBLY

After all electronic components are inserted into a printed circuit board, the first assembly operation is attaching the PC board to the mounting panel using spread tabs. This insures proper alignment of the panel and PC board for module insertion. Once all tabs are through the circuit board, the panel is secured by forming the tabs. Figure 3 illustrates.

The next step is to snap the appropriate module in its panel location. Care should be exercised to make sure the terminals align to the PC board.

107-166-□
SHEET 10

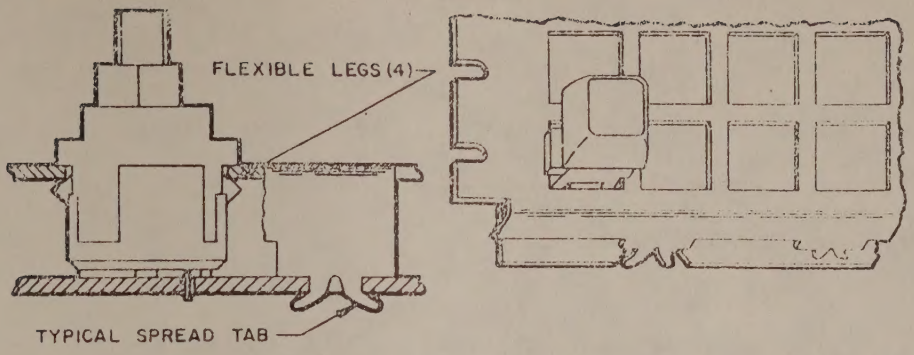


Figure 9
Assembled SD Module

When assembled, the SD module is located within the panel and retained by four flexible legs on the module. The dimensional relationship between the module housing and the mounting hole perimeter allows movement of the module by flexing the legs and provides self-alignment to the printed circuit board. See Figure 9. It is at this point that the retainer pins, if any, are inserted.

WAVE SOLDERING AND CLEANING SD MODULES

Care must be taken during wave soldering and cleaning operation of SD modules. If temperatures exceed certain limits, damage may result from unsoldering the leads from the ceramic sensor pack. Excessive flux in the module will cause operation problems after cleaning.

The SD module must not be cleaned in solvent cleaning systems. The solvents attack the chip potting materials and cause electrical failure.

The following wave soldering and cleaning procedures are the only methods recommended for SD modules.

Wave Soldering

Flux, preheat, solder temperatures and speeds are as follows:

1. Flux - London Chemical Co. - Loncoflux - 106A35X, or equivalent.
2. Preheat - Preheaters should be set to give 200°F (95°C) on top of the PC board just prior to board entering the wave.
3. Solder temperature - 485°F (252°C) maximum, preferably 475°F to 485°F.
4. Speed - Set conveyor speed to approximately 5 ft/min (1,52 meters/min).

Cleaning [Flux Removal]

The flux used for wave soldering is a rosin base flux and is the only one recommended for use with the SD module. Water soluble fluxes are not recommended as they can cause corrosion problems with the finished product.

Generally, there are two types of contaminants on a printed circuit board after wave soldering with rosin base fluxes. The first is an ionized or polar contaminant such as salts, acids or bases deposited on the board during fluxing, handling or printed circuit fabrication. The second is a neutral or non-polar contaminant such as rosin, oil, dust, etc. A satisfactory cleaning operation must remove both polar and non-polar contaminants without further contaminating the assembly.

107-166-□
SHEET 11

The cleaning process recommended here removes all types of contaminants listed.

Detergent - London Chemical Co. - Loncoterge - 446 or equivalent.

Recommended Equipment - Dee Electric Aqueous Cleaner, or equivalent.

Equipment to include the following:

1. Wash Section

   140°F (60°C) maximum water temperature, 5 to 10% maximum solution, low pressure - high volume nozzles. Recommended conveyor speed 3 ft/min. Recirculating tank.

2. Rinse Section #1

   Tap water, not softened, unheated, non-recirculating, low pressure - high volume nozzles.

3. Rinse Section #2

   Deionized water only. Low pressure - high volume nozzles, unheated, and non-recirculating.

4. Air Knife Section

   To remove excessive amounts of water. Note: if the boards do not come out dry, step 5 must follow.

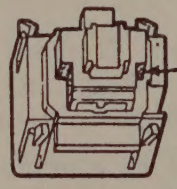
5. Drying Section

   160°F drying for 10-15 minutes, preferably in a non-circulating conveyor oven.

In this cleaning system, the detergent in the wash section removes the non-polar contaminants, the first rinse removes the detergent solution and the deionized water rinse removes the polar contaminants. The air knife and dryer remove all moisture from the assembly so that it can be electronically tested.

Lubrication of SD Modules

To provide reliable module plunger action, SD module plungers should be sprayed with a fluorocarbon lubricant. Recommended is Miller-Stephenson MS-122 aerosol spray, or MS-143 bulk liquid, or equivalent. Both plunger bearing surfaces should be sprayed with a small amount of fluorocarbon lubricant to insure smooth switch actuation. Spraying should be performed after the keyboard has been cleaned and dried.



Shaded areas indicate bearing surfaces to be sprayed.

SPECIAL TOOLS

Special tools are available to assist in keyboard assembly and repair. These tools can be used to easily remove a module or button from a keyboard. Instructions are as follows:

107-166-☐
SHEET 12